SAW Project

Electronic High Performance Components for Applications between 500 and 1000 GHz

Final Report

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Head of Institute	Prof. Dr. G. Tränkle
Project Leader	Dr. H. Yacoub / Dr. S. Boppel/ Prof. Dr. N. Weimann

Authors	Dr. H. Yacoub	Prof. Dr. W. Heinrich
		Dr. K. Nosaeva
		Dr. M. Hossain
		Mr. M. Brahem

Contact:

Ferdinand-Braun-Institut
Leibniz-Institut für Höchstfrequenztechnik
Dr. Hady Yacoub
Gustav-Kirchhoff-Str. 4

12489 Berlin / Germany

Phone	+49.30.6392-2804
FAX	+49.30.6392-2642
Email	hady.yacoub@fbh-berlin.de
Internet	www.fbh-berlin.de

Outline

1 Executive Summary

The project “Electronic High Performance Components for Applications between 500 and 1000 GHz” aimed at establishing a technological base process for realizing not only single components but also integrated circuits for the Terahertz frequency band (from 0.1 to 1 THz). For this purpose, the frequency limits of the InP-HBT MMIC process at FBH were to be pushed towards the 1 THz landmark, by scaling down emitter width and addressing the corresponding challenges in transistor periphery and contacts. Beyond process technology, this included the fields of device modelling, circuit design and mm-wave characterization. In order to verify the achievements within the project, MMICs were to be demonstrated targeting the 300…600 GHz band.

Although the downscaling of the emitter node turned out to be more challenging than anticipated and unexpected problems for basic issues such as f_{max} extraction at very high frequencies had to be tackled, the project achieved a big step towards the 1 THz device, with results close to the intended target specifications. Emitter widths down to 200 nm were realized and, with f_{max} values of 530 GHz and oscillators up to the 500 GHz band, an internationally very competitive performance was demonstrated. Co-operation with the ETH Zürich (Prof. Bolognesi) and the DTU at Copenhagen (Prof. Johansen) was instrumental in reaching this. The results led to a total of 15 scientific publications. They form the basis for ongoing research work at FBH, with the objective to further expand the frequency range of the InP-HBT technology.

2 Introduction

InP heterojunction bipolar transistors, HBTs, offer high frequency operation due to the vertical current transport in their structures. This allows for decreasing the device’s intrinsic transit time by scaling down the total epitaxial thickness.

InP HBTs are normally processed in a quasi-vertical fashion where the emitter, base and collector contacts lie on the same side of the epitaxy. The so called triple mesa process is depicted in **Fehler! Verweisquelle konnte nicht gefunden werden.**. As shown by the figure, the quasi-vertical approach adds to the parasitics of the extrinsic transistor. The increase in collector extrinsic resistance as well as the base-collector capacitance will decrease the maximum frequency attained by such devices.

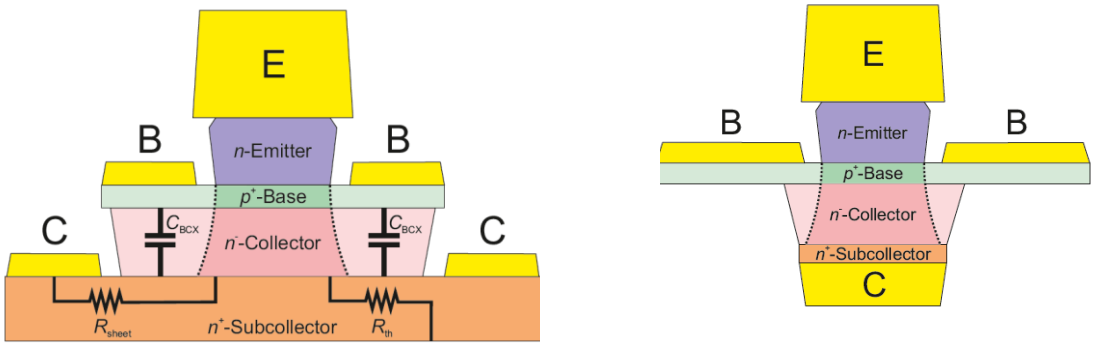

Figure 1: (left) Typical triple mesa process with quasi-vertical collector contact; (right) Transfer substrate method with access to the epitaxy from the back side.

In contrary to the standard triple mesa, the in-house InP HBT process is based on the transfer substrate technique. While the emitter and base contacts are quite similar to those in the triple mesa version, the process deviates when synthesizing the collector contact. Through removing the InP substrate, access to the bottom part of the epitaxy is possible and thus a fully-vertical HBT is realized as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

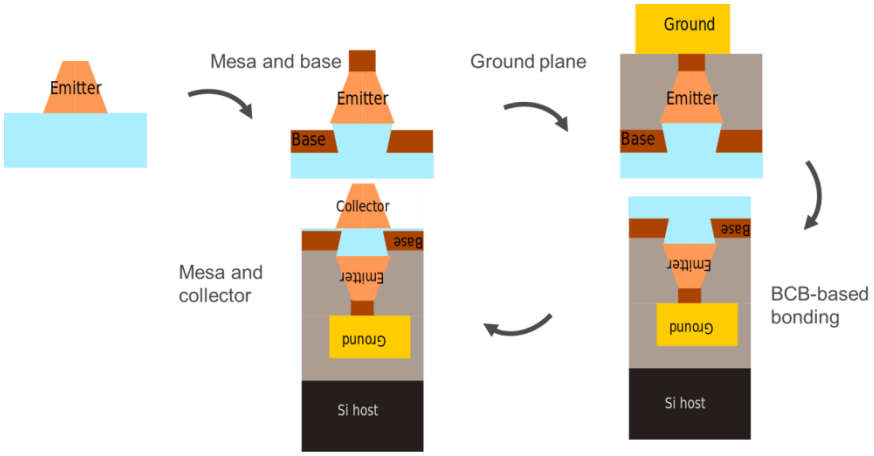

Figure 2: Schematic showing a simplified process flow of the transfer-substrate process.

This allows for the suppression of the parasitic collector access resistance as well as the base-collector capacitance. This means that for the same transistor size, a transfer-substrate HBT will deliver higher transit and maximum oscillation frequencies (f_t and f_{max}) when compared to a triple mesa HBT.

3 Device Scaling for High Frequency of Operation

3.1 Transistor and Epitaxy Simulation

To achieve higher operational frequency, transistor downscaling is inevitable. However, only "shrinking" the dimensions of the transistor without scaling the epitaxy will not yield any significant improvement in the device performance. This requires predictive modelling to simulate the expected performance enhancement when changing specific device and/or epitaxy dimensions.

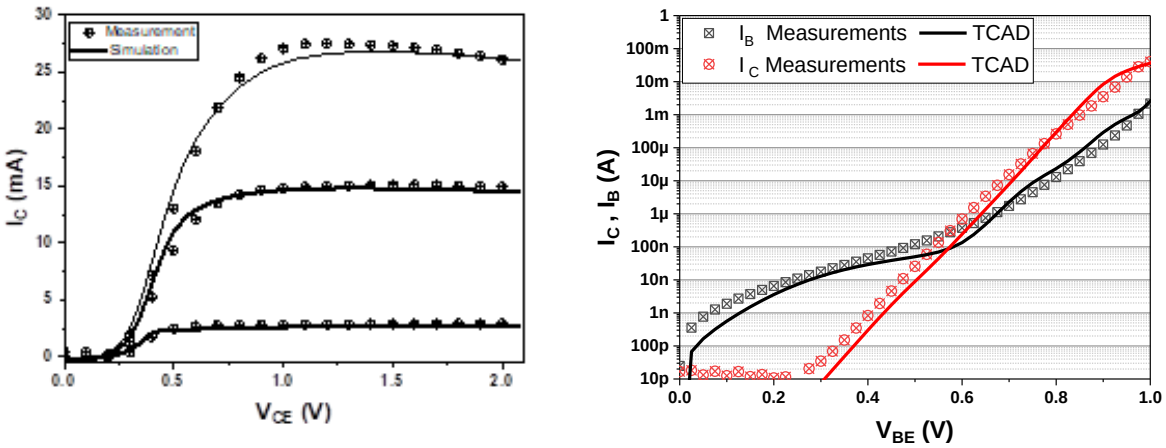

Figure 3: Measured and TCAD-simulated output characteristics (left) and Gummel (right) for a 0.7 µm wide transistor.

To identify current technology bottlenecks, reliable computer-aided design (TCAD) simulations are an integral step. In contrast to the more common lumped-element/empirical approach, the physics based simulation approach offers insight into the dependencies between material and transistor design. Nevertheless, TCAD-based models require rigorous optimization and calibration to reflect the real transistor performance.

Using standard DC and RF measurements, TCAD-models were calibrated taking into considerations parasitic contact resistances, ballistic transport and temperature dependency of carrier recombination and mobility.

Fehler! Verweisquelle konnte nicht gefunden werden. depicts measured data versus TCAD-simulated I-V curves of a 0.7 µm wide transistor processed using the in-house transfer substrate approach. The simulations show good agreement with the measured values indicating proper choice of transport models and correct material parameter extraction. These material models served as the core for the predictive TCAD simulations aimed at downscaling of the transistor dimensions as well as the epitaxy.

To explore the effect of scaling down only the lateral transistor dimensions, TCAD simulations were performed for various emitter sizes. From the two-dimensional TCAD structure, admittance parameters were simulated taking into consideration drift and space charge regions. The simulated admittance parameters were then converted to S-parameters to extract f_{max}. As displayed in **Fehler! Verweisquelle konnte nicht gefunden werden.**, geometry scaling for a standard epitaxial thickness has marginal effect on f_{max}. By scaling down the HBT from 800 nm to 250 nm, f_{max} increases from 350 GHz to about 450 GHz. This confirms that technological node scaling is not enough to achieve the desired transit frequencies. However, by decreasing the thicknesses of the emitter and base in addition to increasing the base doping to compensate for the increased base resistance f_{max} was shown to reach 800 GHz for the same emitter width. The simulations go further and predict that a transistor with an emitter width of 200 nm can provide an f_{max} of 1 THz.

Wafers with the optimized epitaxial stack simulated in **Fehler! Verweisquelle konnte nicht gefunden werden.** were used for processing of the MMIC runs.

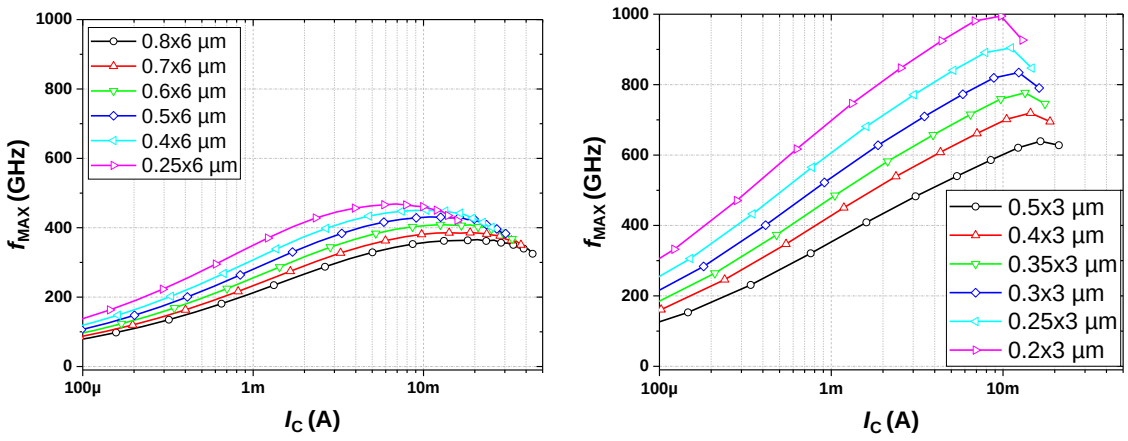

Figure 4: TCAD-simulated f_{max} for different emitter widths with (left) standard epitaxy and (right) scaled-down epitaxy.

3.2 Emitter Width Reduction

Downscaling the emitter size below 500 nm was achieved through developing a new e-beam-based lift-off process. Through utilizing a double PMMA-based process, a resist undercut has been realized applying the same e-beam charge dose. Maximum metal thickness is partially limited by the thickness of the first PMMA layer whereas the upper PMMA layer determines the feature size. The lift-off yield is sensitive to the homogeneity of the resist thickness along with the undercut of the bottom layer of the resist.

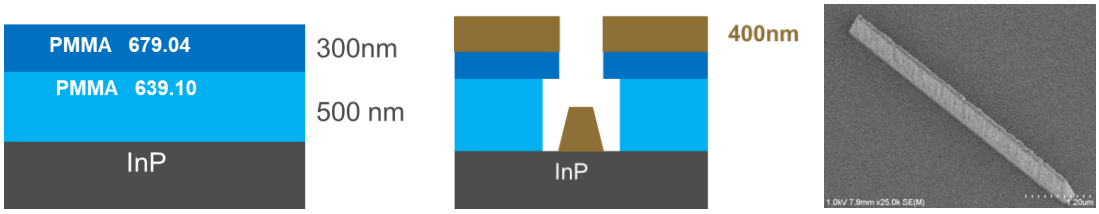

Figure 5: (left and middle) Schematics showing the double PMMA resist process used for emitter lift-off. (right) SEM images of a 200 nm single finger emitter after lift-off process. Notice the tapering of the emitter head with smaller feature size.

To guarantee successful lift-off yield over the whole wafer, PMMA thickness has to be extremely uniform. As seen from **Fehler! Verweisquelle konnte nicht gefunden werden.**, the upper resist thickness is in the order of 300 nm. To achieve thickness homogeneity over a complete wafer, PMMA 679.04 e-beam resist was chosen. Automatic resist coating was tuned to minimize wafer-to-wafer thickness variations. Optimized recipes achieved thickness variations below 20 nm for the bottom resist layer and 7 nm for the upper resist layer.

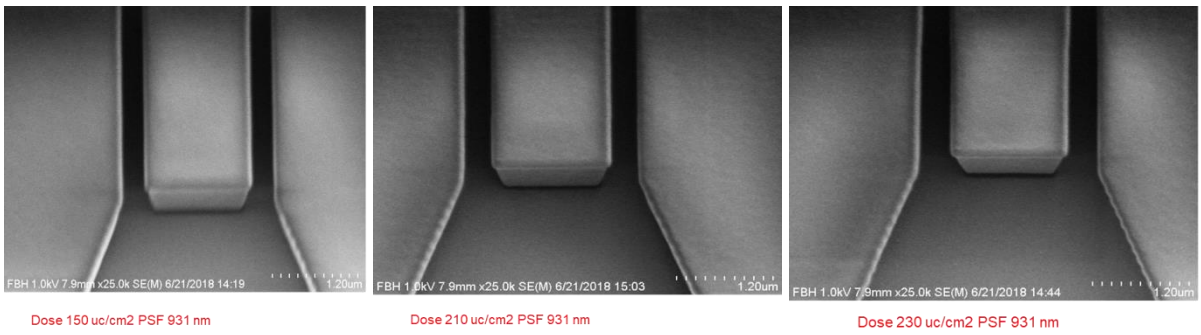

Figure 6: Writing dose variation for the double layer PMMA process.

The E-beam writing dose along with the proximity error correction were also varied to establish a reproducible undercut, which is important for metal lift-off. As can be seen from **Fehler! Verweisquelle konnte nicht gefunden werden.**, a dose of 230 µC/cm^2 has proven to deliver optimum undercut with the required feature size.

3.3 Emitter/ Collector planarization and notch placement

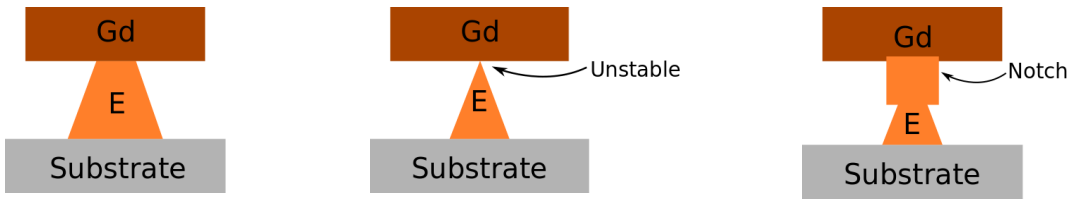

Figure 7: From left to right; Standard emitter size contacting ground metal layer, extremely downscaled emitter size. Notch process for emitter stabilization.

One of the main drawbacks of downscaling of the lift-off process for the emitter and collector is the constant downscaling of the contact area between the emitter and collector to the ground and G1 layers, respectively. To circumvent this problem, an extra notch step is inserted between the emitter (and collector) and the respective galvanic step, which is shown in Figure 7. The notch serves as an extra mechanical stabilizer for the emitter/collector structure without significantly increasing the parasitic capacitance. The effect of the notch

clearance on the increase of the parasitic base-emitter capacitance was simulated using TCAD to enable the design of the required emitter height. As shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**, a notch separation of at least 400 nm has proven to be insignificant with regard to the increase in parasitic capacitance.

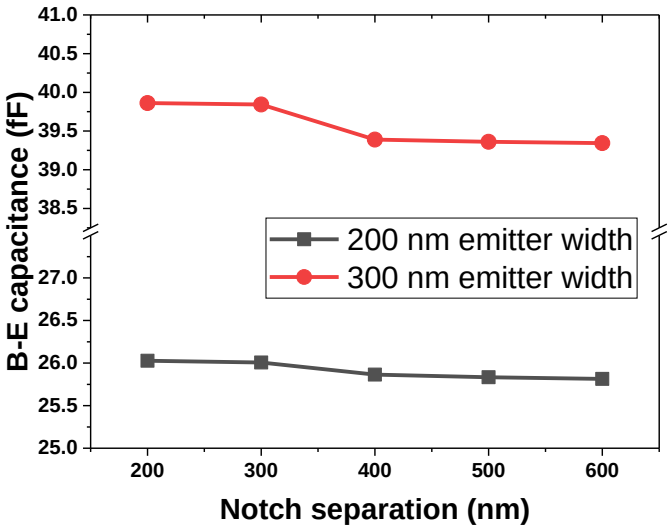

Figure 8: TCAD-simulated base-emitter capacitances for different notch separations for 200 nm (black) and 300 nm (red) emitter widths.

The notch process[1] was developed as illustrated in **Fehler! Verweisquelle konnte nicht gefunden werden.** and 10. The process starts with the planarization of the emitter metal. In this process, at least 100 nm of the emitter head has to protrude from the BCB. Afterwards the lift-off lithography was developed where 500 nm of metal is evaporated to form the notch. A second BCB planarization step is then performed for the protrusion of the notch from the BCB. Finally galvanic metallization takes place to connect the emitter.

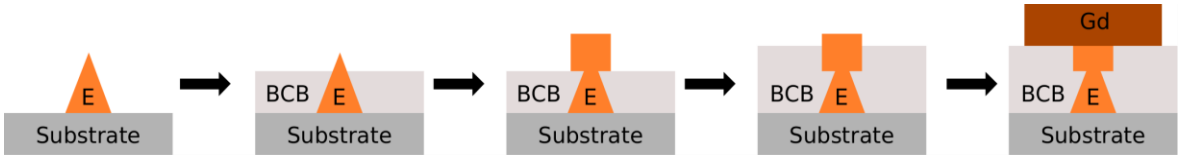

Figure 9: Process flow for notch placement. The process from left to right: Emitter after lift-off, BCB planarization, notch evaporation and lift-off, notch planarization and finally ground metal galvanic.

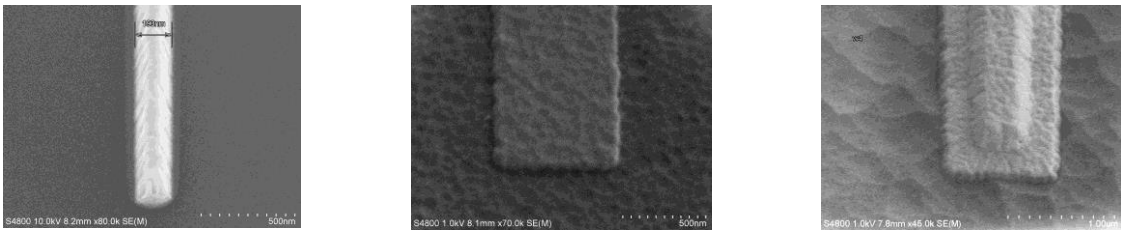

Figure 10: SEM images from the emitter notch process depicting (left) the emitter metal, (middle) emitter after BCB planarization and finally, (right) after notch lit-off.

[1] The collector and emitter notch processes are identical. For the sake of the simplicity, only that of the emitter is mentioned here in text.

3.4 Device Contact Optimization

Pushing transistor frequency limits to the THz range is directly related to the quality of their ohmic contacts and in particular to the base resistance. Hence there is a strong incentive to develop low-resistance ohmic contacts to the p-doped base layer. Pt/Pd-based contacts are the standard metal scheme in III-V device fabrication processes. Previous studies yielded extremely low as-deposited contact resistances, in the order of 2×10^{-8} $\Omega.cm^2$ thanks to uniform and metastable Pdx InGaAs phase formation. Another reported desirable feature of Pd/Pt is the observed penetration or displacement of the native oxide. However, standard Pd/Pt based contacts suffer from long-term stability issues. Metal diffusion and void formation are among the main root causes of contact resistance degradation in InP HBT technology.

Therefore, shallow contacts with stable morphology are required. Refractory metals such as W, Mo, and Ir, are good candidates for a new generation of contacts. These metals have the advantage of lower diffusivity through the semiconductor at high temperature and offer a higher resistance to chemical reaction with the semiconductor when exposed to thermal processing. Ir-based metals were used and tested for long-term stability. During the test the ohmic contacts were annealed at high temperatures of 240 °C (slightly above that of the process thermal budget) for several hours and intermittently measuring the change of the contact resistance. **Fehler! Verweisquelle konnte nicht gefunden werden.** depicts the contact resistance variation over an elongated temperature stress experiment for Pt-based and Ir-based base ohmic contacts. Though both contact types starts predominantly at the same contact resistivity, the Pt-based contacts show approximately 600% increase in resistivity over only seven hours. On the other hand, the Ir-based contacts show a stable behaviour over the same stress time.

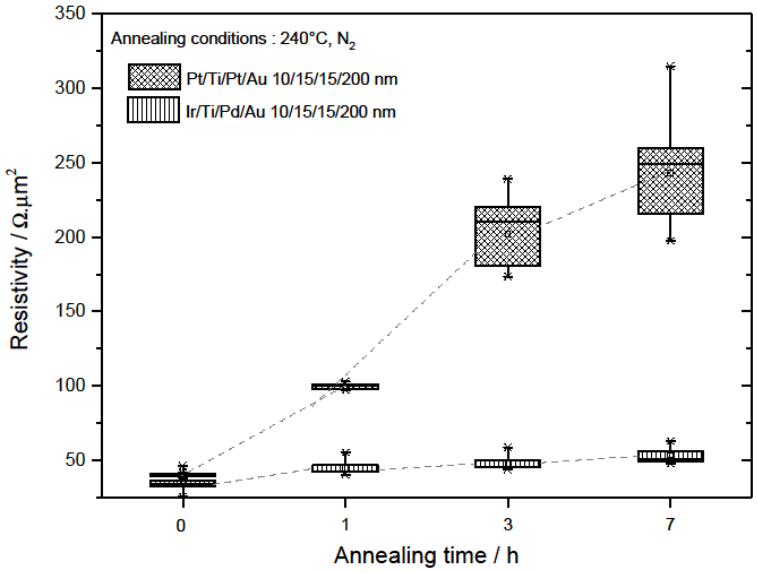

Figure 11: Comparison between the measured contact resistivity of the Pt-based and Ir-based metallization scheme as a function of annealing time. Results are averaged over many samples processed using the same conditions.

To investigate the underlying reasons for the different degradation mechanisms for the two contact types, a microstructural investigation using TEM was performed. The TEM study revealed two major phenomena in Pt-based contacts: (i) extensive void formation in the nearly unreacted region of the platinum layer as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**, and (ii) deep penetration of the platinum into the semiconductor. The voids are assumed to be caused by a Pt flux toward the lower reaction region that is not being balanced by a corresponding flux of group III and group V elements in the opposite

direction. In case of the Ir-based experiment, the contact shows a chemically abrupt interface. An electron diffraction experiment did not reveal any presence of intermixing compounds showing only textured Ir layers (**Fehler! Verweisquelle konnte nicht gefunden werden.**). The out-diffusion appears to be suppressed effectively. No voids in the upper layers were observed, even when annealed for 7 h, demonstrating excellent microstructural stability.

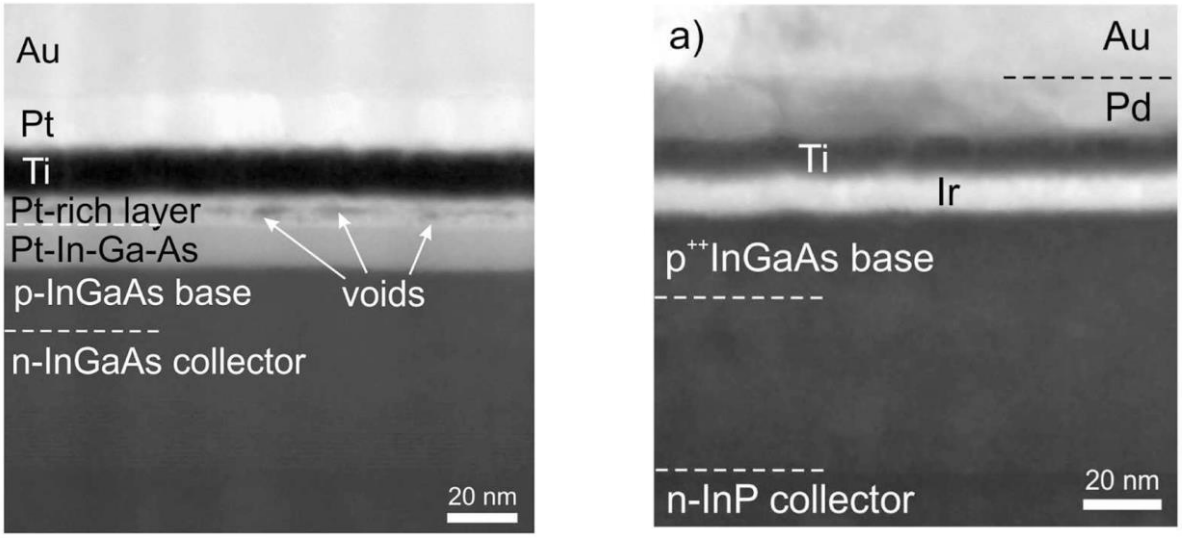

Figure 12: Cross-sectional HAADF STEM micrographs showing (left) Pt-based (right) Ir-based metal stack on InGaAs after annealing at 240 °C for 7 h.

3.5 Thin-film Resistor Optimization

In addition to the high-frequency active components, optimization of the passive components such as resistors and capacitors is very important to achieve a stable MMIC process for THz applications. The thin-film resistor (TFR) is an integral component in each MMIC, from DC-biasing to load/source termination. Stable TFRs enhance not only the circuit performance but also allow for higher design complexity.

Typical TFR representatives are tantalum-nitride (TaN), titanium-nitride (TiN), silicon-chrome (SiCr), copper-nickel (CuNi) and nickel-chrome (NiCr). The most common material is NiCr due to its outstanding properties. Among the above-mentioned materials, Ni(80%)Cr(20%) related to weight percent has the lowest temperature coefficient (TCR) of α=120 ppm/K and the best thermal long-term stability of less than 0.02% degradation after 1000 h at 150 °C.

Hence, the TFRs used in the MMIC process utilize NiCr as the resistive metal. Thickness of the NiCr is kept constant to achieve a constant sheet resistance. By scaling the area of the NiCr, the value of the TFR can be tuned. However, parasitic contact resistance occurs when contacting the NiCr layer to the metallization layers (e.g. G2 galvanic layer). The parasitic contact resistance limits the minimum resistance value achievable by simple scaling rules.

A wet-etching based process has been replaced with a bottom connection lift-off process to achieve lower contact resistance and higher homogeneity over the wafer as displayed in **Fehler! Verweisquelle konnte nicht gefunden werden.**. A specific contact resistance of $8x10^{-10}$ $\Omega.cm^{-2}$ was achieved using the newly developed process decreasing the contact resistance value by almost two orders of magnitude.

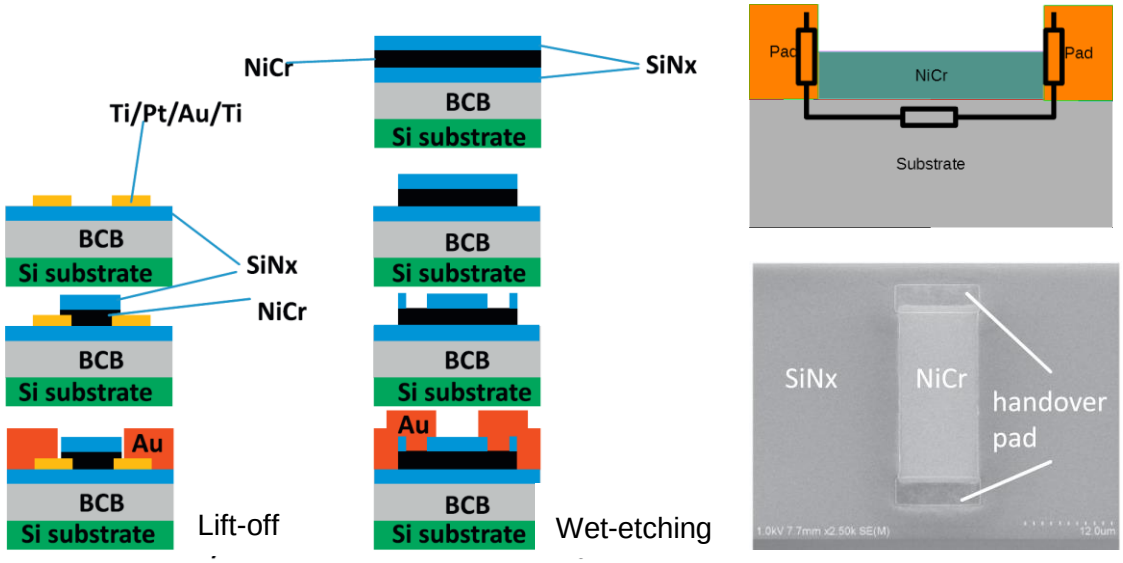

Figure 13:(left) Schematic showing the wet etching and lift-off based processes developed for TFRs. (upper right) Schematic showing equivalent resistive network of the TFR. Parasitic contact resistance occurs when contacting the NiCr films to the metallization layers. (lower right) SEM image showing a NiCr resistor with gold handover pads.

4 Circuit design

4.1 Transistor Model Extraction and Extrapolation

4.1.1 Characterization and Modeling of Medium-Scaled InP HBTs

Interestingly enough downscaled "*THz*" devices are often only modeled and characterized at frequencies well below W-band frequencies. The reason for this is the increased influence from probe-to-probe coupling, multi-mode propagation, and radiation losses which corrupt the measured transistor data. The sensitivity towards de-embedding inaccuracies also becomes larger at higher frequencies. We have investigated how to increase confidence in models extracted using lower frequency data when applied to higher millimeter-wave and THz frequencies. An EM simulation assisted parameter extraction approach for the modeling of down-scaled transferred-substrate InP HBTs has been developed.

The parameter extraction approach is based on the following steps:

- Multiline TRL calibration using on-wafer standards introduced to shift the reference plane to the terminal of the device layout cell
- A distributed external parasitic network determined by calibrated EM simulation
- Extraction procedure applied to the active model following the external parasitic network de-embedding

Fehler! Verweisquelle konnte nicht gefunden werden. illustrates the modeling approach for a 1 × 0.5 × 6 µm^2 emitter size InP DHBT from the ENG2 run.

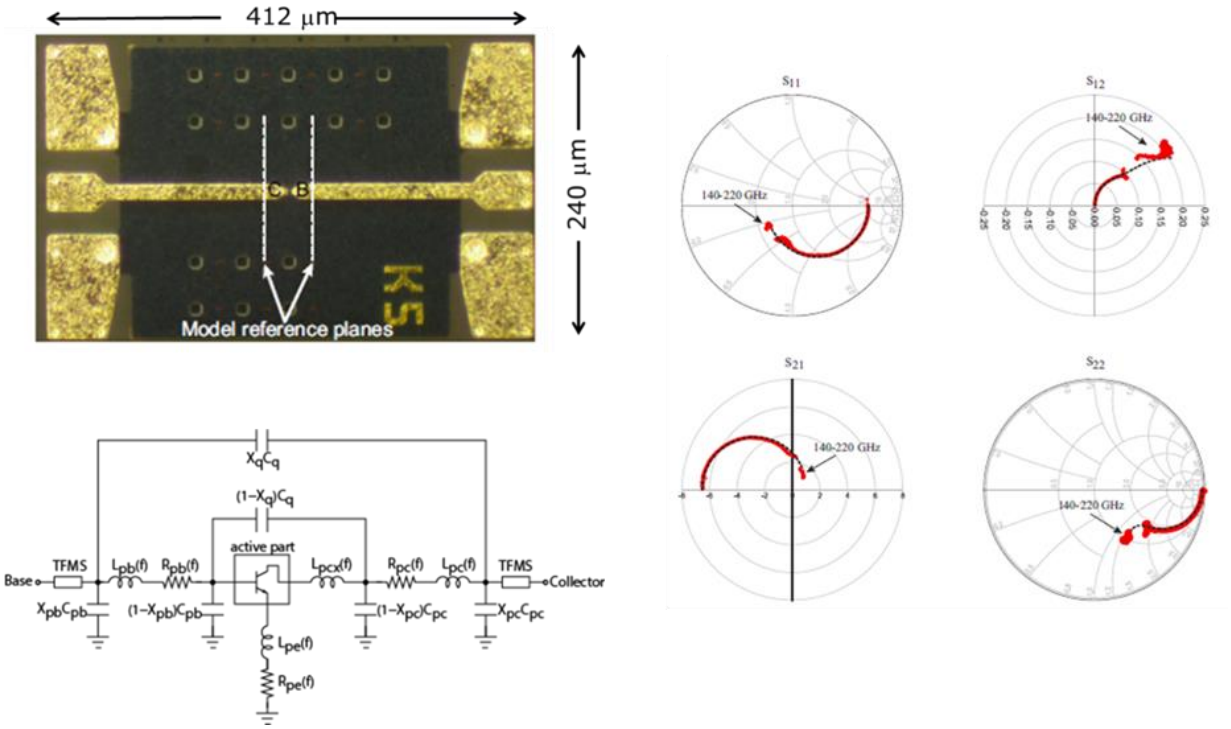

Figure 14: Microphotograph of InP DHBT test-structure in microstrip environment (top right), small-signal model with external parasitic structure (bottom left) and small-signal S-parameters (red symbols - measured, dashed lines – simulated).

4.1.2 Improved de-embedding techniques for characterization of downscaled InP

Unfortunately, once the InP HBTs are downscaled below the limit of 0.5 µm emitter width, artifacts emerge in the unilateral power gain (Mason's gain) for transistors measured in a microstrip environment. These artifacts persist no matter which probes are being used for measurements and for both on-wafer calibration and off-wafer calibration as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**. This makes it very difficult to determine the maximum frequency of oscillation (f_{max}).

On the other hand, it was found that InP HBTs in coplanar environment behaved better, with a clear -20 dB/decade slope in Mason's gain. Improved de-embedding techniques were developed for the transistors in the CPW environment, in particular a de-embedding technique with compensation for the difference between the electromagnetic environment of the on-wafer CPW environment and the calibration substrate. This de-embedding technique is illustrated in Figure 15 and compared to other de-embedding techniques. For a 0.4 µm emitter width InP HBT an f_{max} around 0.53 THz is extracted with good confidence.

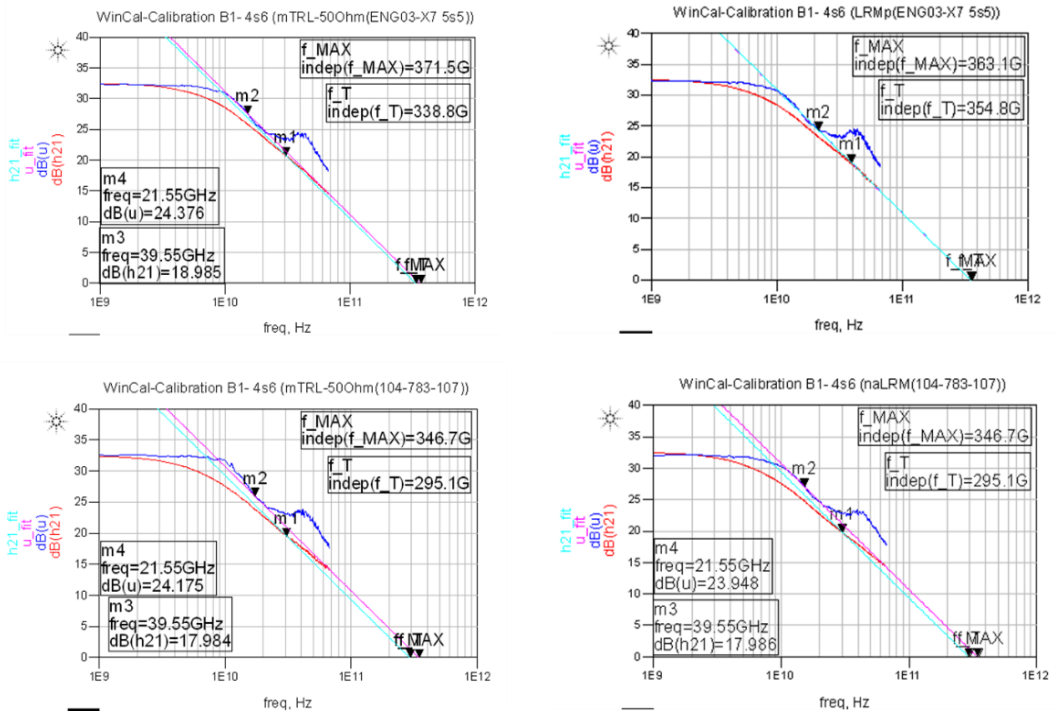

Figure 15: Transistor gains with different calibration approached showing artefacts in Mason's gain.

4.2 Demonstrator Circuit Design

4.2.1 D-band Fundamental Frequency Source

The fundamental voltage-controlled oscillator (VCO) is designed based on a reflection-type oscillator as shown in Figure 16. The circuit uses a single emitter-finger HBT with an emitter size of 0.8 × 5 µm² and an f_t/f_{max} of 350/350 GHz. In order to keep power consumption as low as possible and to achieve the maximum oscillation frequency, the circuit is designed in common-base configuration.

In this oscillator design, the emitter port of the transistor can be used to split up the oscillator into an active and a passive part. The active part of the circuit consists of the transmission lines TLb, TLc1, TLc2 , TLc3 and the HBT, the passive part consists of an open stub and transmission lines TLe with a ground via. A transmission-line section TLb is used to boost the negative impedance seen when looking into the emitter and collector of the transistor (T). In addition, the impedances formed by the lines TLc1, TLc2 and TLc3 on the collector side causes the transistor (T) to become more unstable. To achieve the required oscillation condition in the passive part of the oscillator, the transmission line TLe is used to adjust the phase slope and magnitude. In order to obtain the desired oscillation frequency, an open stub is included at the passive part. All transmission lines are realized as thin-film microstrips.

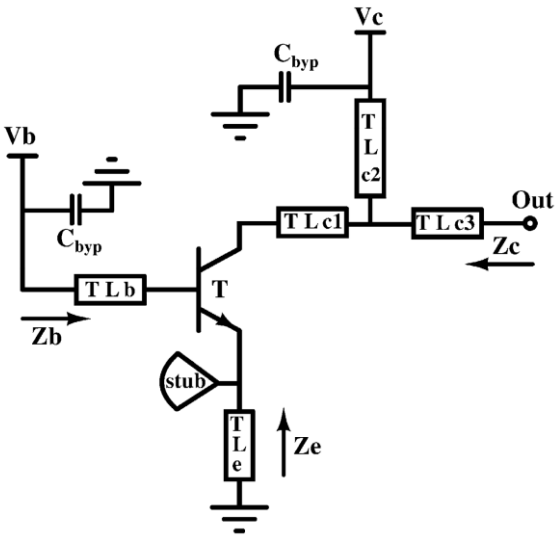

Figure 16: Schematic of the reflection-type fundamental source.

4.2.2 H-band Frequency Source

A push-push oscillator using a 0.3 µm InP TS-DHBT MMIC process was designed for the 500 GHz range based on the transistors models extracted according to the previous section. Due to the compact structure this oscillator can be easily combined to deliver higher output power levels if demanded by the system.

The advantages of push-push oscillators are that they can provide relatively high mm-wave output power and allow for extension of the output frequency close to the maximum oscillation frequency of the transistors or even beyond. The first step was to design a single-ended sub-oscillator in both small-signal and large-signal regime. The sub-oscillator circuit uses a single emitter finger HBT with an emitter size of 0.3 × 5 µm² and f_{max} above 500 GHz. This oscillator uses a Colpitts configuration. In order to keep power consumption as low as possible and to achieve the maximum oscillation frequency, the sub-circuit is designed as a single transistor structure, with the HBT operated in common-base configuration. A transmission-line section TLb1 is used to boost the negative impedance seen when looking into the emitter and collector of the transistor (see Figure 17). The transmission lines are all realized as thin-film microstrip geometries. The impedances formed by the lines TLc1 on the collector and the line TLe on the emitter side cause the transistor to become more unstable and define the steepness of the phase.

To fulfil the oscillation condition, the phase of the reflection coefficient at the emitter port is set to zero by optimizing TLc1 and adding a resonator using a radial stub and a transmission line TLe with a ground via. In this manner, the single-ended sub-circuit (sub osc) configuration is completed. The largest signal swing can be achieved at the collector by directly short-circuiting the differential output, similarly to the drain-connected HEMT push-push oscillators.

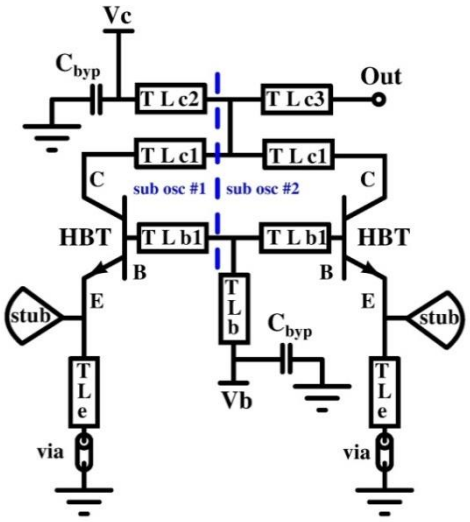

Figure 17: Simplified schematic of the push-push signal source.

5 Technology Runs

For the development of down-scaled devices with increased f_{max}, dedicated technology runs were performed. All those engineering (ENG) processes are based on the Transferred-Substrate (TS) process established at FBH. The key element of TS is an adhesive BCB based wafer-to-wafer bonding with following removal of the InP bulk substrate. In this approach, the active device layers are transferred to a host substrate after the processing of the emitter and base structures is completed. After wafer bonding and InP substrate release, the collector side of the device becomes accessible from the top, allowing for realignment and independent lithographic definition of the collector. Emitter and collector of 0.7µm width are processed using i-line stepper lithography in this case. To downscale the emitter and collector sizes, an e-Beam with a 50 keV shaped-beam system (Vistec SB251) was used for all ENG runs together with all improvements described in Sections 3.2 and **Fehler! Verweisquelle konnte nicht gefunden werden.**.

The epitaxial structures were grown by metal-beam-epitaxy (MBE) on three-inch InP substrates and were commercially acquired. The epitaxy was designed according to the TCAD simulations performed. Emitter and base layer thicknesses were decreased compared to the standard TS process. In addition to the commercially available epitaxy, another type of epitaxial wafers grown at ETHZ (Prof. Bolognesi) by MOVPE were processed. The emitter consisted of $Ga_{0.22}In_{0.78}P$ graded to InP. Moreover, the base was chosen to be GaAsSb for better band alignment with the InP collector.

The schematic of emitter or collector (E1 or K1 layer) metal layer fabrication is shown in Figure 18.

Figure 18: Schematic cross-section of the fabrication of emitter or collector metal layer.

Firstly, the double resist layers are coated on the InP substrate, e-beam exposed and developed with an opening down to 250 nm followed by electron-beam evaporation of the emitter or collector metal stack. The SEM images of one- and two-finger transistors fabricated with e-beam lithography are displayed in Figure 19.

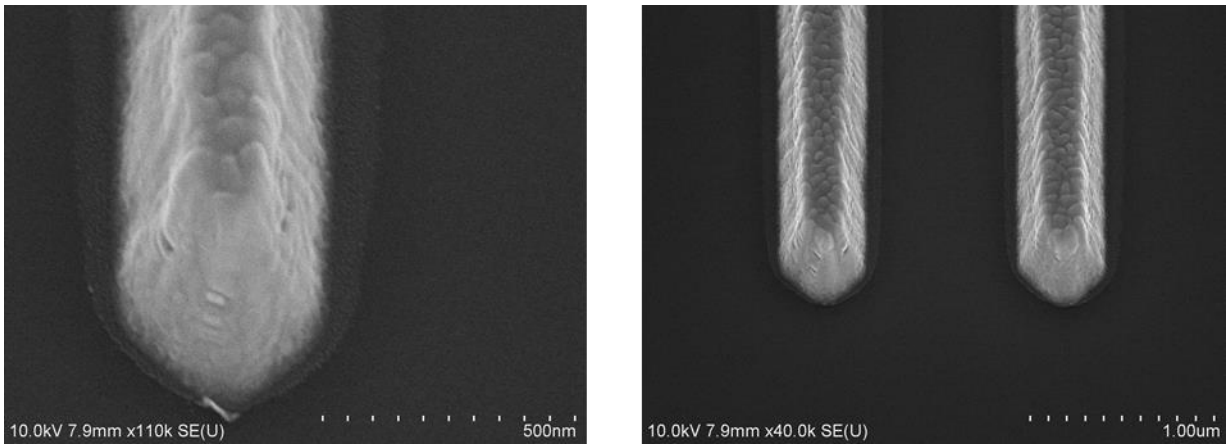

Figure 19: SEM images of one- and two-finger transistor

Afterwards, the emitter mesa is etched using wet chemicals followed by base metal (B1) and base reinforcement metal (BR) evaporation using the same bi-layer resist technology. The SEM images of the finished active part of the transistor on the front side (E1, B1, BR) and back side process (K1) are shown in Figure 20.

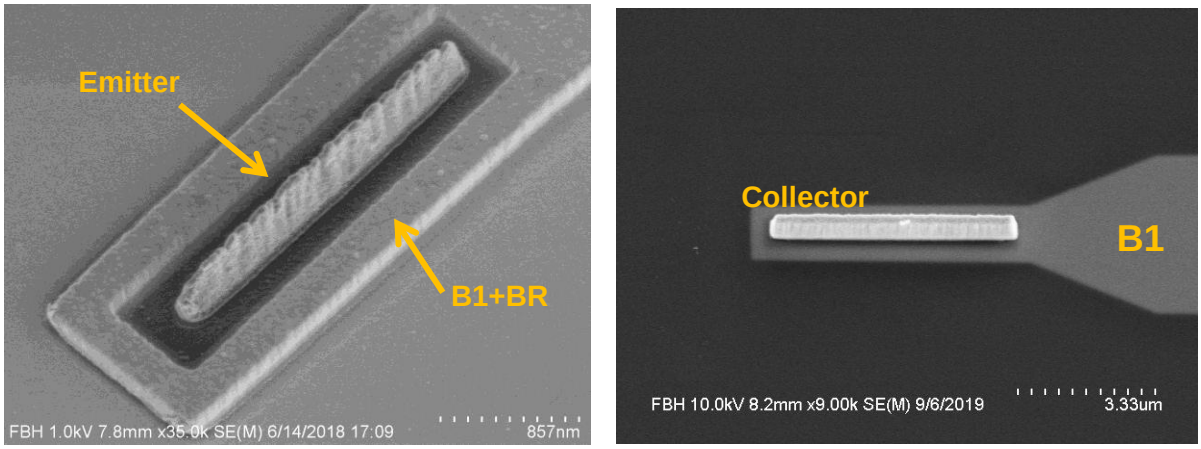

Figure 20: SEM images of emitter, base, base reinforcement metal (left) and collector metal (right) after wafer bonding with subsequent InP substrate removal.

Afterwards, the emitter-base diode is passivated with a SiNx layer by inductively coupled plasma-enhanced chemical vapour deposition (ICPECVD) technique at 80 °C. This has led to significant improvement of device stability as compared to BCB passivation. Following passivation, the surface of the emitter notch is planarized with BCB and 1.5-µm-thick gold is electroplated (first interconnect Gd layer). Then the structure is bonded face-down to ceramic AlN carrier in ENG03 and a thick Si carrier in case of ENG04 using a BCB bond process at 250 °C followed by the wet-chemical release of the InP substrate in hot HCl. It stops on a 200-nm-thick sacrificial InGaAs layer between the InP substrate and the sub-collector layer.

As a next step, the collector metal is placed vertically onto the sub-collector layer using a process similar to that of the emitter, with e-beam lithography with subsequent metal electron-beam evaporation and lift-off. Following device mesa isolation by BCl3 reactive ion

etching, the structure is planarized with BCB. Contact holes are etched in the BCB layer to connect Gd metal and the base metal layer.

The terahertz monolithic integrated circuit process is completed with a 1,5-µm-thick electroplated gold of second interconnect metal G1, a further BCB interlayer dielectric, SiNx thin-film capacitor (0.3 fF/µm^2), NiCr resistor with improved geometry and contact resistance (25 Ω/□) and 4.5-µm-thick electroplated gold of G2 layer. Via V1 connects layers Gd and G1, and V2 connects G1 and G1. An additional via V0 is used to thermally connect RF-grounded areas to the AlN substrates in case of ENG 03 and to the through-silicon-vias (TSVs) in the ENG04 run. A final microscopic image of one of the test transistors is shown below in Figure 21.

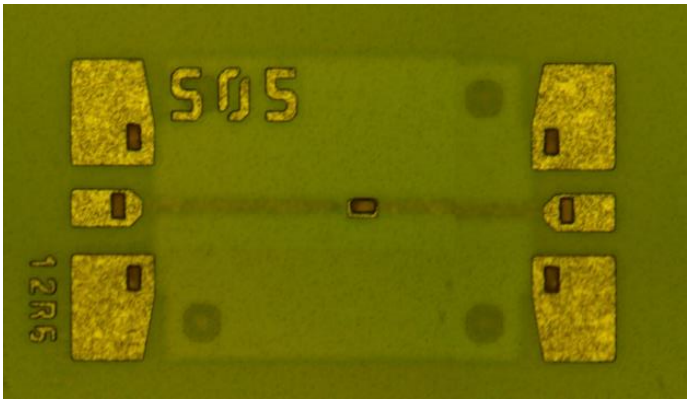

Figure 21: Microscopic image of fabricated test transistor with 0.5µm emitter width.

6 Results and discussion

6.1 Sub-micron transistor performance

The transistors were characterized on-wafer with a standard coplanar probing. DC data were collected with 50 terminated coplanar probe heads. The Gummel plot of a 0.4 × 6 − µm2 device shows a peak current gain of more than 40 as seen in Figure 22. The collector ideality factor amounts to 1.06 in the low-injection regime (Figure 23). The transistor output curve in Figure 22 shows a low turn-on voltage. The negative output conductance at higher current indicates self-heating.

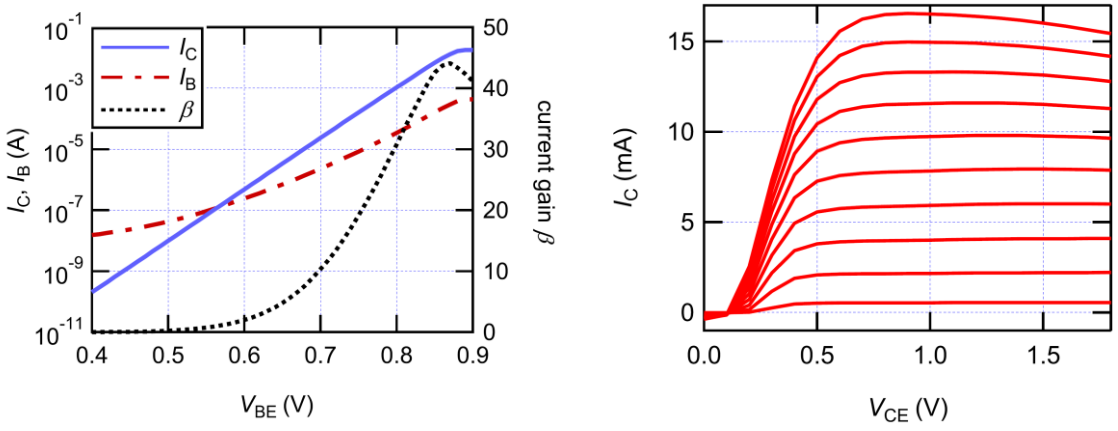

Figure 22: (left) Gummel and (right) output characteristics of 0.4x6 µm^2 transistor

The breakdown behaviour was assessed by measuring the base–collector diode reverse current. The base–collector breakdown voltage of more than 400 transistors was recorded,

defining a breakdown at a reverse current of 1kA/cm2. The distribution of BVCBO is shown in Fig. 23, with a median of 5 V. Short term on-wafer DC stress measurements showed stable transistor performance up to 100 hours, with neither noticeable degradation in the output current nor in the forward current gain.

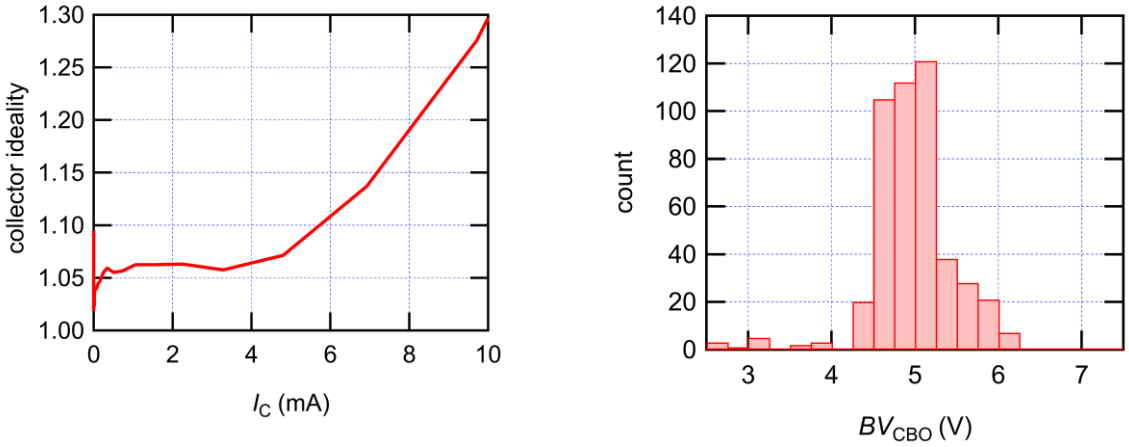

Figure 23: (left) Collector ideality factor and (right) breakdown statistics of an 0.4x6 µm2 transistor.

For RF characterization, the transistors were measured on-wafer using a 110-GHz setup consisting of a PNA network vector analyser (Keysight Inc.) with OML frequency extenders and 100-µm pitch Infinity coplanar probes from Cascade Microtech. The setup was calibrated to the probe tips with the augmented line-reflect-match procedure using an impedance standard substrate (ISS type 104–783) from Cascade Microtech. The bias point for RF extraction was V_{CE} = 1.3 V, IC = 10.5 mA. For accurate estimation of Mason's unilateral power gain at higher frequencies, a distributed de-embedding approach was employed as discussed in Section 4.1.2. Current gain and Mason's gain extracted from de-embedded s-parameters are depicted in Figure 24. f_t and f_{max} values of 370 and 535 GHz, respectively, are achieved.

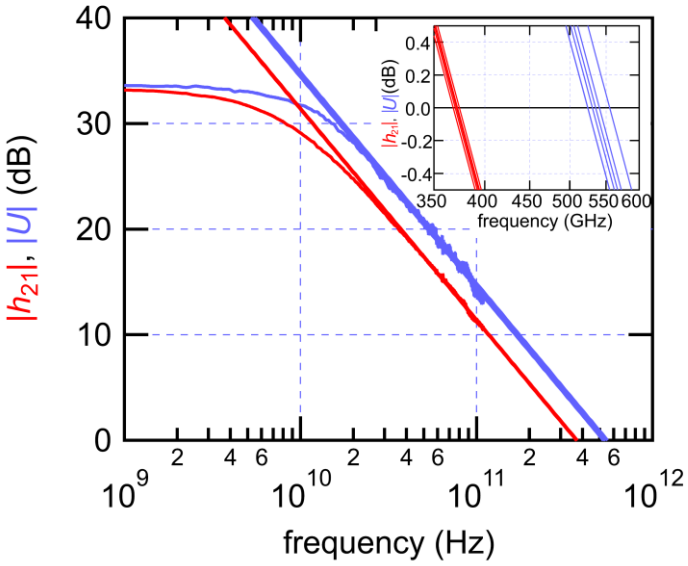

Figure 24: Current gain (h21) and Mason's unilateral gain versus frequency.

6.2 D- and H-band Sources Performance

Both chips were fabricated using the newly developed sub-micron MMIC process. The fabricated D-band and the H-band sources had chip areas of 0.65x0.6 mm² and 0.85x0.75 mm², respectively. Figure 25 displays microscope images of the fully fabricated MMICs. The chips have ground-signal-ground RF input ports with 50 µm pitch size. DC bias was supplied via external DC probes with alternating bias and ground pads.

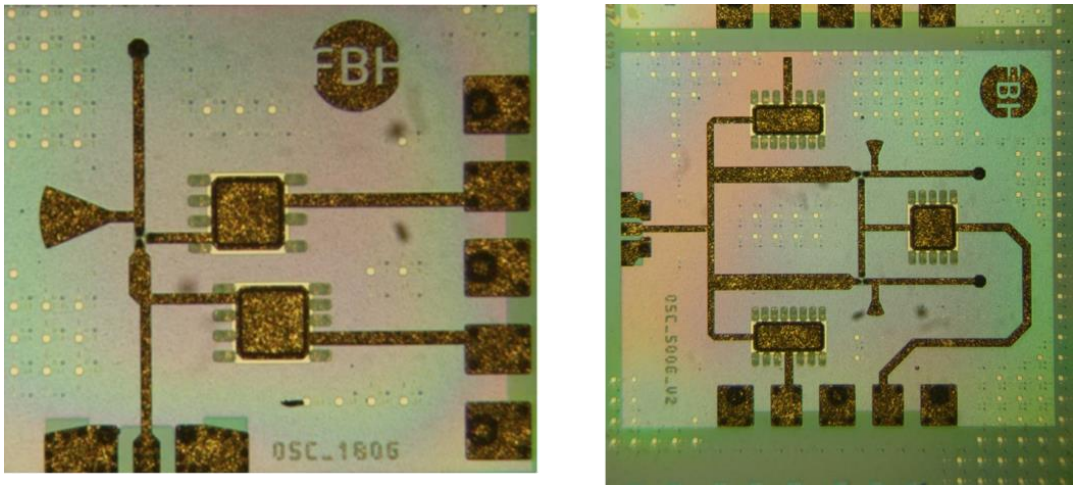

Figure 25: Optical microscope images of (left) D-band and (right) H-band source MMICs.

6.2.1 D-band Source

Characterization of the signal source was performed in two major steps: First, the oscillation frequencies with tuning range as well as phase noise were determined. A WR5 waveguide probe with a sub harmonic mixer (SHM) from RPG was connected to the output. The down-converted signal was measured using a R&S FSW spectrum analyser.

The second step was to measure the peak power of the circuit. A WR5.1 GSG waveguide probe was connected to a 90-degree WR10 bend and taper, which lead to the input of a power sensor and an Erickson PM4 power meter. The insertion loss of the output probe is 2 dB as specified by the vendor and the waveguide bend and tapers are estimated to contribute a total insertion loss of 1.5 dB in the desired frequency band.

Accordingly, the measured output power values need to be corrected by +3.5 dB to account for the losses of probe, waveguide extension, and tapers. Thus, one arrives at an actual peak output power of 9.5 dBm at 146 GHz. The DC power consumption is only 43.5 mW from a 2.5 V power supply, which corresponds to 20 % DC-to-RF efficiency. The frequency tuning is achieved by varying the base current in the range 0.25 – 0.6 mA. This allows a tuning range of about 2 GHz (1.4 %). **Fehler! Verweisquelle konnte nicht gefunden werden.**, the output frequencies of the source and DC-to-RF efficiency as well as the output power are plotted as a function of the base tuning current.

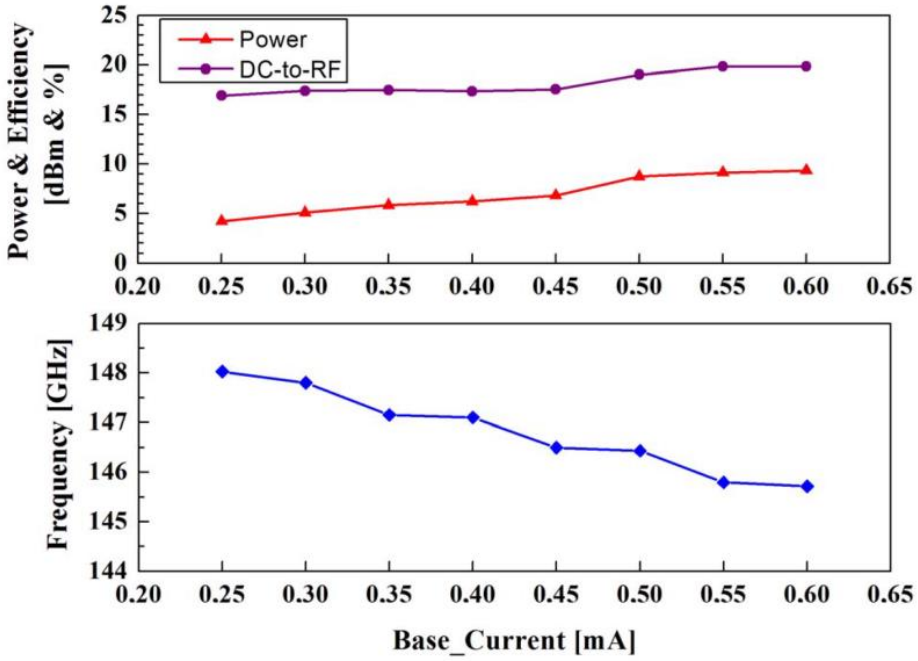

Figure 26: Measured output power, DC-to-RF efficiency and frequency of the source as a function of the base tuning current (waveguide and prober loss de-embedded).

6.2.2 H-band Source

The circuit was characterized on-wafer. A ground-signal-ground (GSG) T500-S-GSG-50-BT WR2.2 waveguide probe (Form Factor) and a WR2.2 sub-harmonic mixer (SHM) from Radiometer Physics (RPG) were used to extract the output signal. A precision voltage source was employed for DC supply. The down-converted signal was measured using a spectrum analyser from R&S. **Fehler! Verweisquelle konnte nicht gefunden werden.** presents raw data of measured output power spectrum. Special care has to be taken in order to ensure that the correct spectral component is evaluated. This was verified using the spectral position of individual harmonics and sideband signals. An accurate phase noise measurement using a spectrum analyser at such high frequencies is very difficult, due to the impact of the down conversion mixer and local oscillator purity. An actual peak output power of -11 dBm at 480 GHz. Additionally, DC-to-RF efficiency is plotted when tuning the base voltage. The DC power consumption is only 15 mW from a 1.6 V power supply, which corresponds to 0.5 % DC-to-RF efficiency.

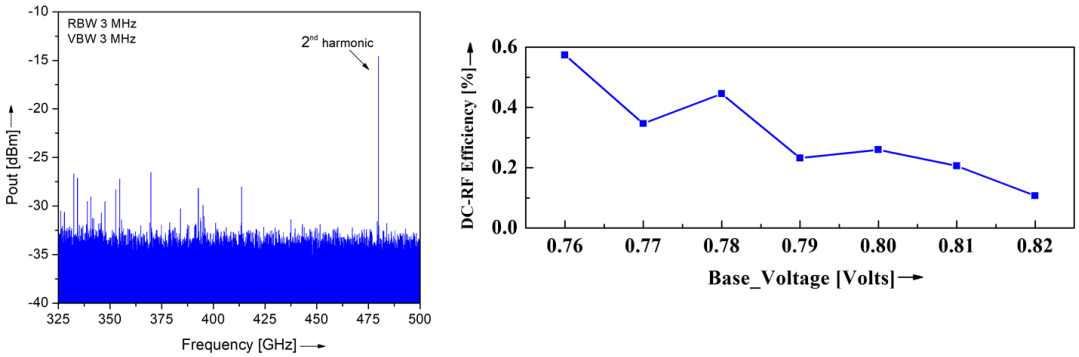

Figure 27: (left) Measured output power spectrum, (right) measured DC to RF efficiency.

Fig. 28 adds measurement data on output power and frequency as a function of the base voltages used for tuning.

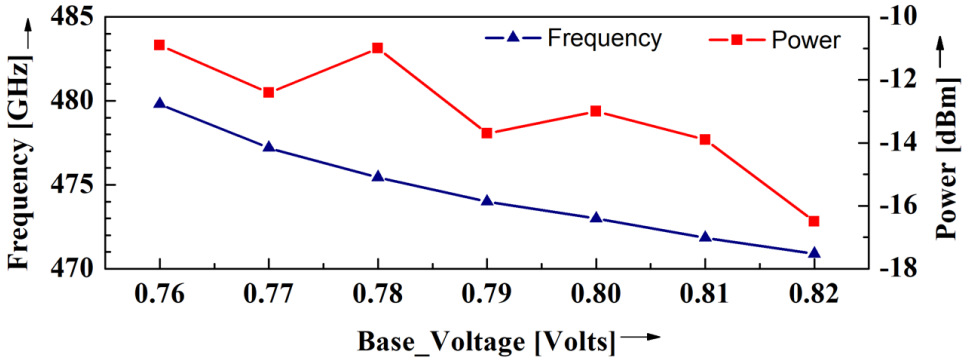

Figure 28: Measured output power and frequency versus tuning voltage as the base.

7 Conclusions

The main scientific and technical achievements of this project can be summarized as follows:

- Technological advancement for deep sub-micron scaling of the InP HBT process was achieved, emitter widths down to 200 nm were realized. This was coupled with TCAD-aided material design in order to push the transistor performance towards the 1 THz target.
- Transistor parameter extraction, especially regarding f_{max}, was improved in order to cover the down-scaled devices with sufficient certainty.
- Maximum transit frequencies f_{max} of 530 GHz for devices with a 400 nm emitter within an MMIC process were reached. This compares well with the international state of the art, as is shown in Fig. 29 (see scaling line).

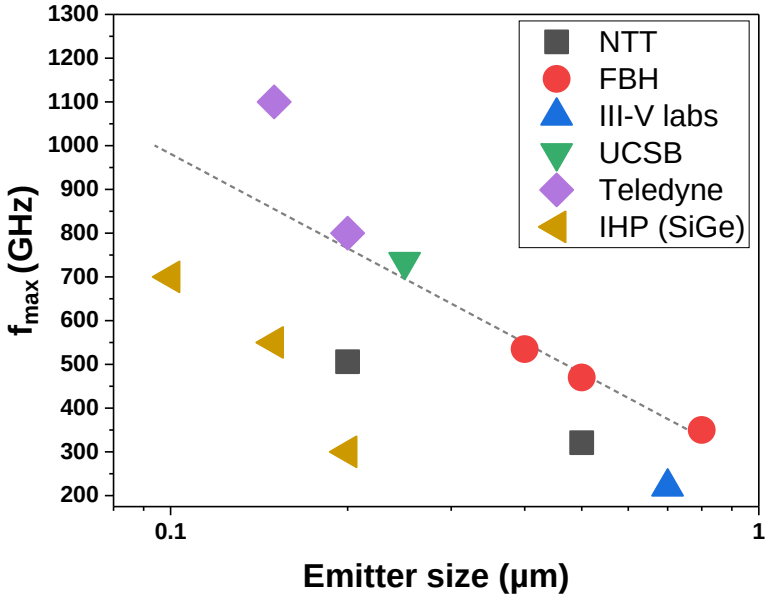

Figure 29: F_{max} as a function of emitter size benchmarking the FBH process to the state of the art of InP processes and SiGe-HBTs.

- Multiple process modules have been optimized and newly developed to reach a stable and high-yield MMIC process. This included transistor modules improvement as well as passive components.
- The performance of the MMIC process was demonstrated with oscillator circuits at in the 150 GHz and 500 GHz frequency range. Output powers of 10 dBm at 148 GHz and of -11 dBm at 480 GHz, respectively, were achieved.
- The new process versions developed in the course of this project are the subject of ongoing work at FBH in order to further push the frequency limits of the InP HBT technology.

8 Scientific Co-operation

The project has greatly benefitted from two international scientific co-operations:

- With Prof. Colombo Bolognesi from Swiss Federal Institute of Technology in Zürich (ETHZ) in the field of HBT epitaxy. The GaAsSb epitaxial wafers, on which the maximum frequency of 530 GHz was achieved, were grown at ETHZ.
- With Prof. Tom K. Johansen from the Technical University of Denmark (DTU) at Copenhagen. Prof. Johansen contributed greatly in the parameter extraction and the model development of the InP HBT.

9 Publications

The results were published in a total of 15 papers and conference contributions, among them 6 journal publications and 5 refereed presentations at the two internationally leading microwave conference events.

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[2] M. Hossain, N. Weimann, M. Brahem, O. Ostinelli, C. R. Bolognesi, W. Heinrich, and V. Krozer, “A 0.5 THz Signal Source with -11 dBm Peak Output Power Based on InP

DHBT," in *2019 49th European Microwave Conference (EuMC)*, 2019, pp. 856–859, doi: 10.23919/EuMC.2019.8910876.

[3] M. Brahem, A. Mogilatenko, D. Stoppel, D. Berger, S. Hochheim, D. Rentner, I. Ostermay, M. Reiner, S. Boppel, K. Nosaeva, and N. Weimann, "Thermally stable iridium contacts to highly doped p-In0:53Ga0:47As for indium phosphide double heterojunction bipolar transistors," *Microelectronic Engineering*, vol. 215, p. 111017, Jul. 2019, doi: 10.1016/j.mee.2019.111017.

[4] N. Weimann and W. Heinrich, "THz InP Integrated Heterojunction Bipolar Transistor Technology for mm-Wave Beam Steering Applications," IMS 2019, Workshop WMH-2, Boston, MA, 2019.

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[9] M. Hossain, M. H. Eissa, M. Hrobak, D. Stoppel, N. Weimann, A. Malignaggi, A. Mai, D. Kissinger, W. Heinrich, and V. Krozer, "A Hetero-Integrated W-Band Transmitter Module in InP-on-BiCMOS Technology," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, 2018, pp. 97–100, doi: 10.23919/EuMIC.2018.8539915.

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Antennas, Communications and Electronic Systems (COMCAS), 2017, pp. 1–4, doi: 10.1109/COMCAS.2017.8244768.

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