Leibniz-Gemeinschaft

Final report

# Science Fab for hetero-integrated InP/BiCMOS high-frequency systems

Leibniz-Institute: Leibniz-Institut für innovative Mikroelektronik (IHP)
Reference number: SAW-2013-IHP-3
Project period: 01.01.2013 – 31.12.2016
Contact partner: Dr. Marco Lisker

# Final Report SAW Project

# Science Fab

# (SciFab)

**IHP, Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder)**

**In cooperation with**

**Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Berlin**


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Reference: SAW-2013-IHP-3

Project duration: Jan. 1, 2013 to Dec. 31, 2015

## Contents

*Executive Summary*

The SciFab project had the goal to co-integrate Indium Phosphide (InP) double heterojunction bipolar transistors (DHBTs) together with Silicon-Germanium (SiGe) bipolar and complementary metal oxide semiconductor BiCMOS technologies by using a wafer-to-wafer permanent bonding process. The targeted applications were mmw-wave circuits with output frequencies above 100 GHz covering divers areas like wireless communication, security scanners, material quality control, robotic and machine vision, spectroscopy, or medical imaging. In addition to the previous HiTek project one focus point of the SciFab project was the improvement and homogenization of the process modules.
Another more essential objective of the project was the development of a complex design environment to make the heterogeneous integrated InP-DHBT on SiGe BiCMOS technology accessible for circuit designer from universities, institutes and industrial customers from small and medium enterprises. Finally the partners wanted to offer the new developed heterogeneous technology in a multi project wafer (MPW) manner. To share the semiconductor R & D and fab cost over a diverse market, a foundry model is most suitable.

Further developments compared to the former Leibniz-SAW project “HiTek” of the process modules necessary for the hetero-integration were achieved during the three runs realized in the project time span. The improvements are the decrease of step height in topography prior to wafer bonding, the simplification of alignment marks formation and the avoidance of oxidation of the top metal surfaces to simplify the contact generation between InP metal system and SiGe BiCMOS back end.
Another relevant issue which was solved was the establishment of a common design environment.
In the first phase of this project a definition of the design kit requirements was developed.
Due to the marginal influence of the hetero-integration on the SiGe devices the transistor models for the SiGe devices in the design kit remain valid. The design kit was extended to include the models of the InP HBTs and passives included in the BCB – gold back-end-of-line stack of the InP technology.
The InP active and passive devices were added during the SciFab project to the already existing Keysight ADS design kit. As a result of the SciFab-project hetero-integrated circuits can be developed in schematic capture. The schematics are synchronized with the layout including all technology layers of both the InP DHBT and the SiGe BiCMOS stack. A Design Rule Check (DRC) is installed and functional. A complete ADS Momentum stack that includes all routable metal layers of the combined technology is incorporated.

Combined BiCMOS and InP integrated circuits using SciFab technology have been designed using the combined design kit and successfully realized during the project lifetime. The results of the measurements on these circuit demonstrators were published in journals and on international conferences.

The SciFab foundry admittance is facilitated over IHP’s multi-project-wafer MPW user interface. Potential customers can request the design kit from IHP as the tool kit for designing their own circuits. Circuit building blocks are also available on request. Design submission is equal to IHP’s BiCMOS procedures – customers submit their final GDS file and after checking the layouts the wafer preparation is started at IHP followed by the processing at the FBH. The requested number of chips is shipped after the completion to the customer. The SciFab InP/BiCMOS heterogeneously integrated foundry is currently operating in an early access mode with a selected number of external customers.

## 1. Motivation and Objectives

In the semiconductor industry the most established platform are silicon based technologies as the key component for the impressive rise of digital circuits and the use of complementary metal oxide semiconductor field effect transistors (CMOS FETs). Over decades the scaling of the CMOS devices followed Moore's law and the aggressive scaling leads to very small devices with gate length in the range of some tens of nanometers with operating voltages of approximately one volt. For analogue purposes the frequency performance of the devices is a key element. The cut-off frequencies $f_T$ and $f_{max}$ were increased continuously over the last years. But the increase of the unilateral power gain cut-off frequency $f_{max}$ which is a useful parameter since it is directly related to the power amplification [Mason 1954], is limited for CMOS devices.

The highest $f_{max}$ value measured for silicon-based devices were measured on heterojunction bipolar transistors (HBTs) constructed from Si-SiGe-Si vertical structures with frequencies of $f_{max}$ 570 GHz at room temperature [Boeck 2015]. Currently there are further developments ongoing to achieve even higher $f_{max}$ values up to 700 GHz [Lachner 2014]. With respect to maximum operating voltages different breakdown voltages like open base emitter-collector breakdown voltage $BV_{CE0}$ and the base -collector breakdown voltage $BV_{CB0}$ have to be considered. These SiGe-HBTs show $BV_{CE0}$ of approximately 1.6 V.

Alternatively III/V compound semiconductors with higher band gaps and higher mobility of its charge carriers can deliver higher breakdown voltages at a similar or even better frequency performance. A high electron mobility transistor with 25 nm gate length [Mei 2015] shows the highest $f_{max}$ values exceeding 1.5 THz and they are based on indium phosphide (InP). But also InP HBTs with narrow emitter windows of 120 nm width show $f_{max}$ values of more than 1 THz [Hacker 2013]. The breakdown voltage of InP devices at these high frequencies show nevertheless higher values than the SiGe HBTs. For example the breakdown voltage $BV_{CE0}$ of an InP HBT with $f_{max}$ of 900 GHz still exceeds 4 V [Rode 2015].

A figure of merit to compare different transistors fabricated in different technology platforms and from diverse material systems is the product of $f_{max}$ x $BV_{CE0}$. A large number of different semiconductor devices systems are shown in Figure 1. It ranges from scaled CMOS technologies for processor circuits including billions of transistors up to GaN-based power amplifiers with a few transistors in the complete circuit. The Si-based devices usually have a low value of the product $f_{max}$ x $BV_{CE0}$.

The GaN HEMT devices have the highest product $f_{max}$ x $BV_{CE0}$ resulting from the enormous breakdown voltages reaching up to hundreds of volts [Xi 2011, Ren 2015].

However, indium arsenide (InAs) channel material in the InP HEMT, and the indium gallium arsenide (InGaAs) or gallium arsenide antimonite (GaAsSb) base material of the InP HBT exhibit higher electron mobilities and velocities than GaN. Therefore, InP devices enable a higher $f_{max}$ as GaN based devices.

The challenge of the III–V semiconductors is the technology and process platform to realize complex integrated circuits, represented in the number of transistor in a circuit (x-axis in the Figure 1).

The lower possible complexity of InP technologies is caused by the small integration density reached up to now. A combination of these III/V- and CMOS based technologies in multi-package systems might be a solution to combine the benefits from both sides. But such package solutions are cost intensive and multi-package system implementations suffer from coupling losses.

Heterogeneous integration of different semiconductor technologies can overcome these restrictions. Such a technology can offer a platform construction kit for any particular (sub-) circuit application. The Idea is to integrate all RF components required for a RF transmitter, consisting usually of baseband processor, local oscillator, up-conversion mixer, power amplifier, and possibly a frequency multiplier on one chip.

There are different approaches to do a hetero-integration of III/V semiconductors on silicon. One is to grow the epitaxial III/V material on the silicon with different materials as buffer layers to do lattice matching [Kazior 2011]. But this method is expensive and the risk of contamination of the Si devices is a given circumstance. An integration of the InP devices or circuits on the top of the silicon would be a choice to avoid any contamination risks. A chiplet assembly was reported recently using a bumping for connecting the Si and InP circuit parts [Gutierrez-Aitken 2010]. The accurate adjustment and interconnect are the challenges here. Another approach was reported by the use of a wafer-to-wafer bonding process were the electrical connections between the Si CMOS devices and the InP HBTs were realized after bonding [Royter 2009].
The asterisks in the diagram (Figure 1) represent the device parameters (products of cut-off frequency by breakdown voltage) and the maximum number of transistors in one circuit of the technologies offered by both institutes (IHP and FBH). The red ellipse symbolizes the BiCMOS technology, where SiGe HBTs and pure Si CMOS are co-integrated already. The SciFab leads to a seamless combination of both technologies with a large benefit for mm-wave-circuits and systems.

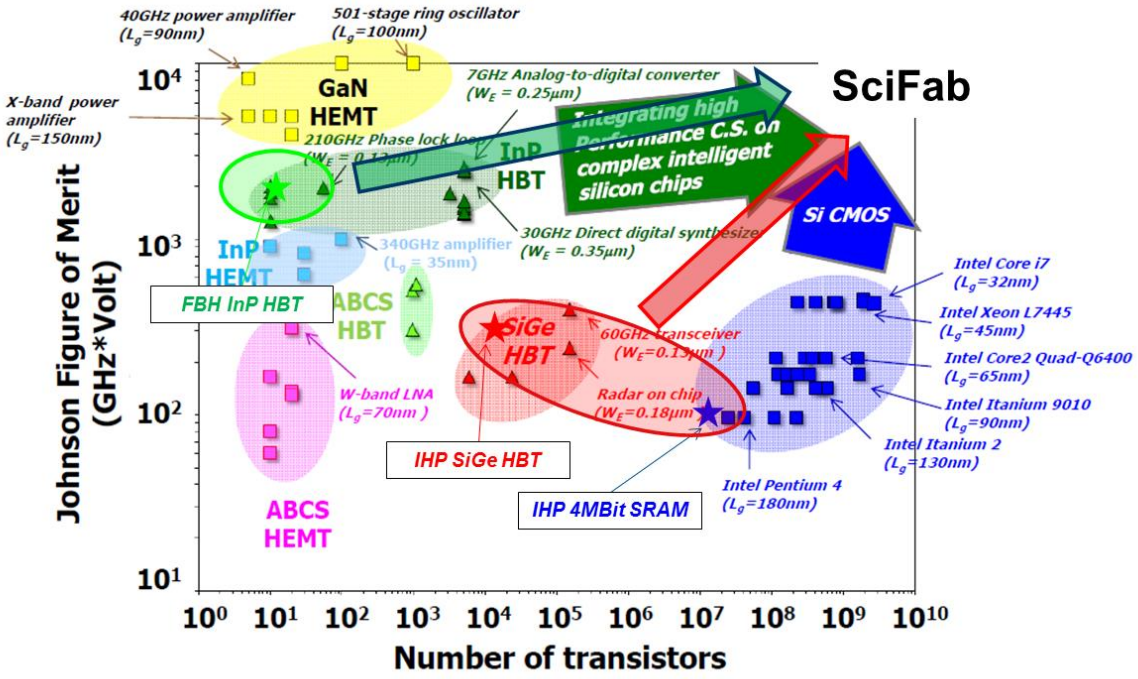


**Figure 1: Johnson Figure of Merit vs. Number of transistors for different semiconductor material systems**

In the SciFab project the goal was to co-integrate Indium Phosphide (InP) double heterojunction bipolar transistors (DHBTs) together with Silicon-Germanium (SiGe) bipolar and complementary metal oxide semiconductor BiCMOS technologies by using a wafer-to-wafer permanent bonding process. In addition to the former project HiTek one focus point of the SciFab project was the improvement and homogenization of the process modules.
Another more essential goal of the project was the development of complex design environment to make the heterogeneous integrated InP-DHBT on SiGe BiCMOS technology accessible for circuit designer from universities, institutes and industrial customers from small and medium enterprises. Finally the partners want to offer the new developed heterogeneous technology in a multi project wafer (MPW) manner.

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## 2. Progress of work

Further improvements compared to the former Leibniz-SAW project "HiTek" of the process modules necessary for the hetero-integration were achieved during the three runs realized in the project time span. The improvements are the decrease of step height in topography prior to wafer bonding, the simplification of alignment marks formation and the avoidance of oxidation of the top metal surfaces to simplify the contact generation between InP metal system and SiGe BiCMOS back end.
Another relevant issue which was solved was the establishment of a common design environment.
In the first phase of this project a definition of the design kit requirements was developed. The InP active and passive devices were added during the SciFab project to the already existing Keysight ADS design kit. As a result of the SciFab-project hetero-integrated circuits can be developed in schematic capture. The schematics are synchronized with the layout including all technology layers of both the InP DHBT and the SiGe BiCMOS stack.
A Design Rule Check (DRC) is installed and functional. A complete ADS Momentum stack that includes all routable metal layers of the combined technology is incorporated.

Combined BiCMOS and InP integrated circuits using SciFab technology have been designed using the combined design kit and successfully realized during the project lifetime.

## 3. Results

### 3.1 Design Kit

The name of the developed InP DHBT on SiGe BiCMOS heterogeneous integrated technology in this project is "SG25InP1" and represents the "SciFab" technology. The hetero-integrated technology is based on a qualified 250 nm BiCMOS technology already existing at the IHP for several years with InP as an add-on.
As the baseline technology for the project we choose a standard 0.25µm-SiGe-BiCMOS technology (SG25H1). As described in the papers [Lisker 2014, Kraemer 2014] and the SAW final report from the HiTek Project [Heinrich 2013] the InP is added onto the BiCMOS by an permanent bonding process with subsequent remove of the InP substrate including devices specific for this particular InP technology available at the FBH.
The BiCMOS technology supplies two types of high-performance HBT transistors with slightly different values for peak $f_T$ and $f_{max}$ ranging from 180 GHz up to 220 GHz. [1]The parameters of the HBT transistors are summarized in the following table (Table 1).

[1] At the end of the project the H1 technology was replaced by the H4. SG25H4 consists of the same electrical devices like in SG25H1 but with a more advanced design environment.

The npn2 has a narrower emitter window $d_E$ = 0.18 µm compared to npn1. This transistor has higher values for $f_T$ and $f_{max}$. The breakdown voltage $BV_{CEO}$ is 1.9 V for both transistors whereas the dc current gain □ is higher for the npn1 transistor.
These two types of npn-bipolar-transistors are also usable in the combined circuits of SG25InP1.
The SiGe-BiCMOS-technology includes CMOS devices consisting of n-MOS and p-MOS transistors useable for digital designs like signal sources, controllers and memory circuits.

**Table 1: SG25H4 npn HBT transistor parameters also available in SG25InP1**

| SG25H4 | npn1 | npn2 |
|---|---|---|
| $A_E$ | 0.21 x 0.84 µm² | 0.18 x 0.84 µm² |
| Peak $f_{max}$ | 190 GHz | 220 GHz |
| Peak $f_T$ | 190 GHz | 200 GHz |
| $BV_{CE0}$ | 1.9 V | 1.9 V |
| $BV_{CB0}$ | 4.5 V | 5.0 V |
| $V_A$ | 40 V | 40 V |
| ß | 270 | 260 |

In the SciFab runs the digital part was used to build PLL (phase-locked loop) control systems which were necessary to create VCOs with temperature independent output frequency as a useful demonstrator. The parameters of CMOS FETs are summarized in the following table (Table 2). The devices were tested before and after the waferbonding process and the subsequent finalization at the FBH clean room to ensure a sufficient small influence of these processes on the devices parameters.

**Table 2: CMOS parameter included in the hetero-integrated technology**

| | | SG25H3/H4* |
|---|---|---|
| **Core Supply Voltage** | | 2.5 V |
| **nMOS** | $V_{TH}$ | 0.6 V |
| | $I_{OUT}$** | 540 µA/µm |
| | $I_{OFF}$ | 3 pA/µm |
| **pMOS** | $V_{TH}$ | -0.6 V |
| | $I_{OUT}$ | -230 µA/µm |
| | $I_{OFF}$ | -3 pA/µm |

* Parameters for SGB25V are similar
** @ $V_G$ = 2.5 V

Passive devices like resistors and capacitors as well as inductors are also included.
A short overview is given in the following table (Table 3):

**Table 3: Parameters of passive devices included in the hetero-integrated technology**

| | SG25H3/H4 |
|---|---|
| MIM Capacitor | 1 fF/µm2 |
| N+ Poly Resistor | 210 Ω/□ |
| P+ Poly Resistor | 280 Ω/□ |
| High Poly Resistor | 1600 Ω/□ |
| Varactor Cmax/Cmin | 3 |
| Inductor Q@5 GHz | 18 (1 nH) |
| Inductor Q@10 GHz | 20 (1 nH) |
| Inductor Q@5 GHz | 37 (1 nH)* |
| * with LBE | |

The design kit was developed to give designers the opportunity to use the available devices in a proper way. The development of the SG25InP1 design kit was one of the main goals of the project.

All the BiCMOS active and passive devices are included in the Keysight ADS 2012 design kit. The InP devices were added during the SciFab project. Now a combined design can be developed in schematic capture (Figure 2).
The circuit diagram symbols are connected with the layout including incorporated layers of both the InP DHBT and the SiGe BiCMOS-technology. Layout Verification and Design Rule Check are working. Predefined cells for transistors and passive devices (capacitors and thin-film resistor) coupled with the InP module are incorporated.

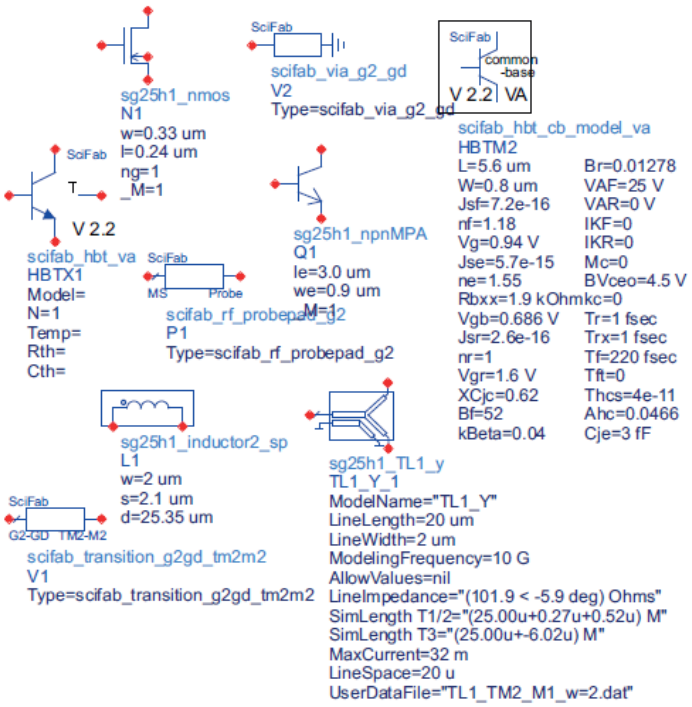



**Figure 2: Devices of both InP and SiGe layer stacks are included. (screenshot of ADS schematic capture)**

### 3.2 Process Module Improvements

Within the SciFab project some major improvements of the technology development were achieved by different wafer processing cycles. The process flow is devided in three parts. First the 200mm Si wafer is processed in the clean room of the IHP. The wafers pass through the standard SiGe-BiCMOS process flow until they reach the passivation module. Here some modification were necessary to enable the bonding process. The first modification was the increase of the TiN layer on top of the TM2 stack as discribed in chapter 3.2.1 to avoid the formation of aluminum oxide. The TM2 planarization is decribed in 3.2.2 followed by explanations about the back-side alignment marks in section 3.2.3. and finaly the 3” wafer dicing in chapter 3.2.4. The infrastructure of the IHP allows the completion of the BiCMOS lot(s) within 3 months.

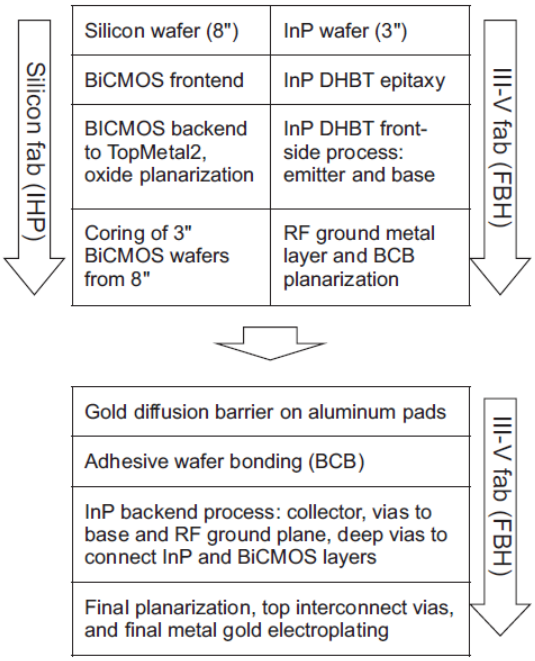



**Figure 3: SciFab process flow in both institutes**

In parallel the production of an InP lot with 3” diameter is staretd at the FBH. The InP DHBT process uses comercial vertical structures of solid-source molecular beam epitaxy (SSMBE) InP-wafer.
An epitaxial regrowth is not required after the bonding process. Moreover epitaxy steps are impossible after bonding due to thermal budget limitations to 250 °C caused by the existence of benzocyclobutene (BCB) at this stage of manufacturing (Figure 3).

The InP wafer was processed with all front-end-of-line processes and already has one metal level of gold, the ground metallization (Gd) with benzocyclobutene (BCB) as the dielectric when it comes to the bonding process. At this stage the front-to-front wafer bonding process is performed (see Figure 4 a). The ground metallization (Gd) of the InP wafer is embedded in BCB. Prior to wafer bonding both wafers are spin coated with “bonding” BCB (see Figure 4). After a BCB curing the two wafers are aligned and bonded. After the bond process the InP substrate is dissolved by HCl to expose the InP DHBT structures (see Figure 4 a). The vias between the InP and SiGe-BiCMOS structures are formed by inductively coupled plasma (ICP) RIE dry etching through the BCB using SF6. Then they are electrically connected using a gold electroplating process. The deposition of BCB as inter layer dielectric (ILD) by spin coating and the deposition of gold and definition by Lift-Off technique is repeated several times to define the Metal levels G1 and G2 and also the vias inbetween (see Figure 4 b).

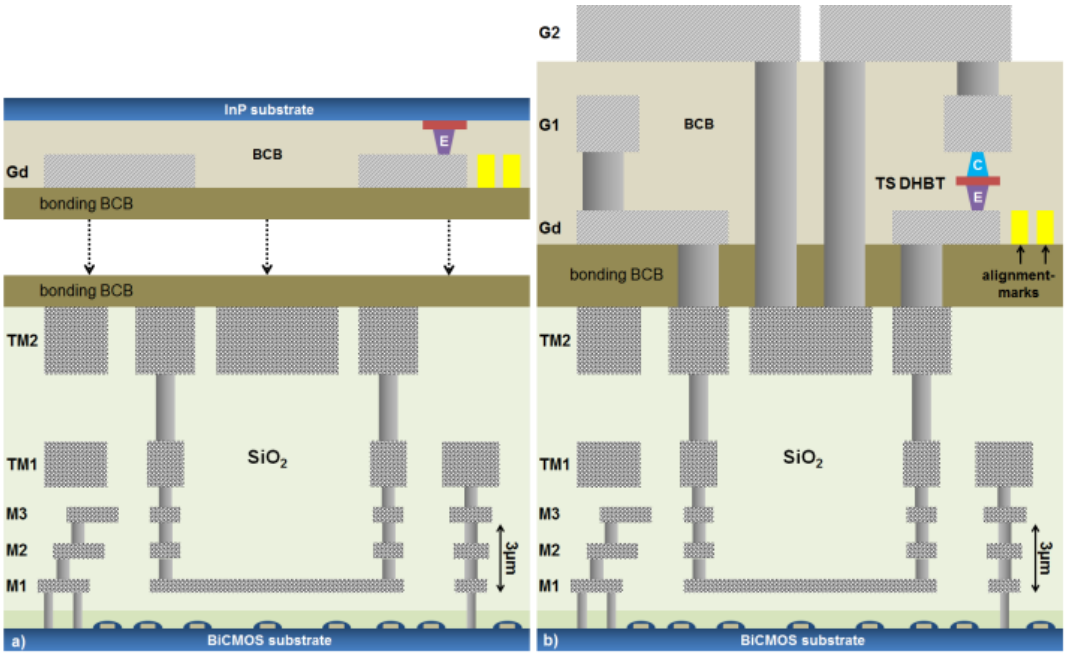



**Figure 4: InP-on-BiCMOS substrate transfer process: InP and silicon wafer are bonded using BCB as glue (a). After the InP substrate removal by HCl further processing takes place. The interconnects between TM2, Gd, G1, or G2 are produced to form RF interconnections. Additional metal layers G1, G2 and the corresponding via levels between G1, G2 and Gd are deposited using gold plating (b).**

The complete technology flow consists of a stack with 8 metal levels. Five aluminum based in BiCMOS part and three of gold in the InP section. The InP-DHBTs are located in between metal Gd and G1, refer to Figure 4.

### 3.2.1 Top-Metal 2 stack – contact resistance to Au metal system

In IHPs BiCMOS part there were some modifications necessary compared to the standard 0.25 µm BiCMOS technologies. First of all a planarization of the top most metal level (top metal 2 = TM2) was necessary. It was described in [Lisker 2014]. The Hitek final report [Heinrich 2013] and Ostermay [Ostermay 2014] metioned the formation of “purple plague” and an interfacial insulating layer caused by the existence of an aluminum oxid layer on top of the TM2 pads. This aluminum oxid is formed after exposing the TM2 to ambient atmosphere. This unwanted oxidation was observed especially at the wafer edges of the 200 mm wafers. As a definition of the bonding requirements an exposion of the TM2 was agreed. Since the standard TM2 stack has a 30 nm thick TiN layer on top and due to the inhomogenieties of the processes in combination with the enormous oxide thickness of 6500 nm after the deposition the removal of the TiN at the wafer edge is unpreventable. To avoid this disrupting oxide the thickness of the TiN was increased to 120 nm (see Figure 5). No Aluminum is exposed on any point of the wafer and accordingly no oxidation occurs.

### 3.2.2 Top-Metal 2 planarization CMP process without SiN stopping layer

Both wafers need to fulfill stringent requirements in terms of low surface step heights. This is the reason why the top metallization (TM2) of the BiCMOS wafer needs to be planarized. It is performed by the deposition of silicon dioxide using high-density plasma HDP and TEOS-based plasma-enhanced chemical vapor deposition PECVD, with subsequent chemical-mechanical polishing (CMP) and dry etching. The HDP Oxide is used because of its good gap fill capabilities. After the CMP process, which stops when global wafer planarization is reached, the residual $SiO_2$ on top of the metal is removed using mask-less dry etching. The etching works with endpoint detection realizing the exposure of TiN of the TM2 metal stack

(refer to Figure 5). Therefore, we can achieve a step height below 100 nm across the wafer from the metal structures to the surrounding SiO2 dielectric, which is very important for the wafer bond process later on.

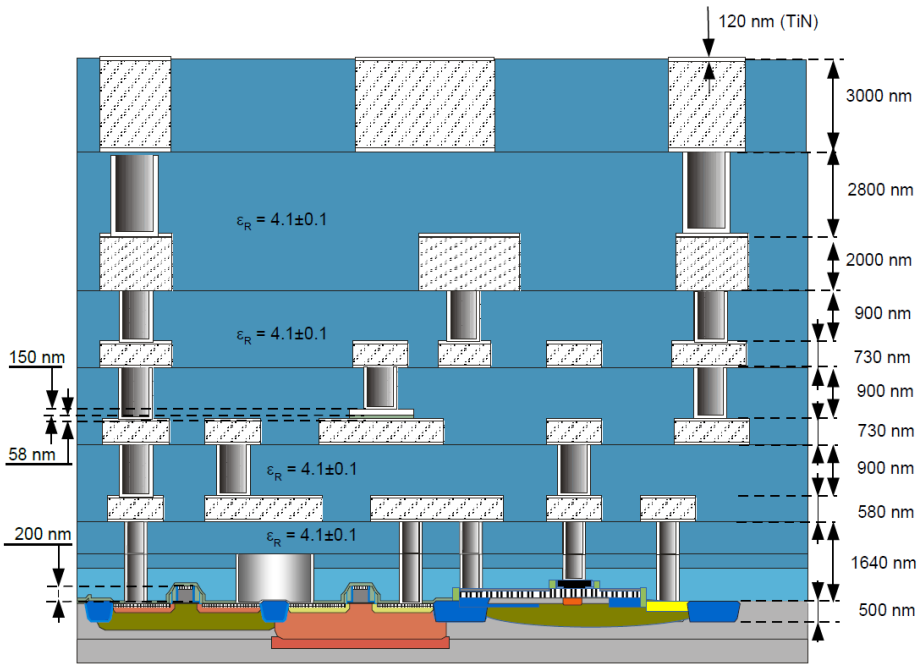



**Figure 5: Cross section scheme of the complete SiGe BiCMOS with planarized TM2 and 120 nm TiN on top of the metal stack (not to scale)**

### 3.2.3 Simplification of the Generation of alignment marks on the Si-wafer back-side

Alignment marks are required to perform an accurate permanent wafer bonding. The bonding was realized with benzocyclobutene (BCB). Additional metal layers and vias have to be assembled after the bonding process to connect the BiCMOS devices with the InP DHBTs. An accurate landing on the top metal of the BiCMOS metallization system is essential to ensure the function of the hetero integrated circuits.
An EVG420 alignment tool was used for the pre-bond alignment at FBH. Since the wafer pair is opaque for visible light and will be bonded front-side to front-side and this tool has just one lens, alignment marks are needed on the front side of one wafer and on the back-side of the other wafer. Alignment marks were prepared on the back side of the silicon wafer. We used standard back side lapped wafers which are ineligible for back side lithography because of their roughness. Therefore a back side planarization process had to be developed. CMP was used to realize the planar back side required. The standard back side lapped wafers were chosen instead of back side polished wafers because of possible handling issues with those backside polished wafers in the clean room tools. The back side planarization is carried out after the deposition of the oxide on top of TM2, so the metal pads are protected by 6.5 µm of silicon oxide.
The lithography on the back side was performed using a Nikon NSR-SF150 i-line lithography tool. The tool has the opportunity to perform an aligned exposure on the back side because the wafer is transparent for infrared light. These marks were etched into the silicon surface of the back side with a depth of some hundreds of nanometers using reactive ion etching method.
After the etching and cleaning steps the misalignment to the front side was measured using an EVG40NT overlay tool. The tool consists of a front and back side microscope (two lenses) that allows the evaluation of overlay errors. The alignment errors were less than 0.3 µm.

### 3.2.4 The wafer sawing process

Since the post bonding process takes place in the 3” InP process line at FBH and the Si wafer is a 200 mm wafer a sawing process is necessary. A number of four 3” silicon BiCMOS wafers can be cut out of one 200 mm wafer. The pre-defined die size for the SG25InP1 designs is 10.38 x 10.38 $mm^2$. This corresponds to the best trade-off for the different requirements (Lithography, wafer size) of both technology environments. The sawing process was performed using an automatic dicing tool DAD3350 from Disco with a special sawing blade able to do circle cuts. After the aligned definition of the 3” wafer a main flat was sawed with a length of 22 mm. Finally the wafer bevel was emulated using a special 45° blade. The bevel has a width of 200 µm all around the wafer and also along the flat. The wafer was flipped for beveling the edge of the back side. The bevel is necessary to avoid the formation of particles during the handling in and out of the plastic wafer carriers in the process steps after the wafer bonding.

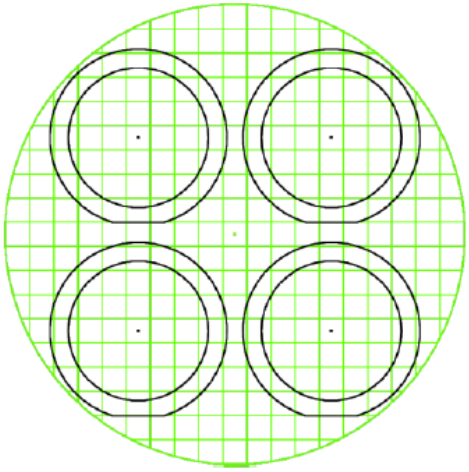


**Figure 6: Four 3“-diameter wafer cored out of one 200 mm-diameter silicon wafer**

### 3.3 Impact of the heterogeneous integration on the BiCMOS devices

The influence of the heterointegration on the performance of the BiCMOS devices was carefully evaluated. A block of test structures for all kinds of CMOS devices, HBT transistors and passives like metal-insulator-metal (MIM) capacitors is incorporated in every die of IHP’s MPW runs. These standard test structures (so called “process control monitors” PCMs) are the basic devices of the technology (HBTs, CMOS, resistances, capacitors, etc.). It is very important to control the values of the device parameters during the production and after finalization to ensure a stable processing and high yield.
The first electrical characterization is performed after finalization of metal 1 (M1), to examine that the front-end-of-line processes worked properly. Almost all transistor parameters except the frequency parameters $f_T$ /$f_{max}$ and some yield related PCMs are determinable at this stage.
After completion of the standard BiCMOS preparation an additional electrical measurement is performed. Every electrical parameter of the devices is accessible at this point of manufacturing including the transit frequency $f_T$ and the maximum oscillator frequency $f_{max}$ of the hetero-junction bipolar transistors.

Additional steps were introduced for the heterogeneous integration flow with InP as described in the chapter before. Additional measurements were performed after the bonding process and the finalization of the whole BCB/gold metallization stack. A high functionality and a high yield of the hetero-integrated circuits are desired.

### 3.3.1 DC parameters of the CMOS transistors

A set of parameters was used for the characterization of the CMOS devices. They were measured at ten different MOSFET test structures for each channel carrier type. There are n-channel and p-channel transistors included with different geometric dimensions. The measurements were carried out in a checkerboard arrangement (every second die) because of the 290 dies on a 200 mm wafer.
A number of electrical parameters are measured for different MOS transistor structures reflecting the output and transfer characteristics of the particular MOS device. Main parameters are the threshold voltage VT, the effective gate width WEFF, the effective gate length LEFF, the drain induced barrier lowering DIBL, the source-drain current at enhanced state at VDS=VGS=2.5V IDS25, and at 1.8V IDS18, the off-current IL25 and IL18, as well as the sub-threshold slope.

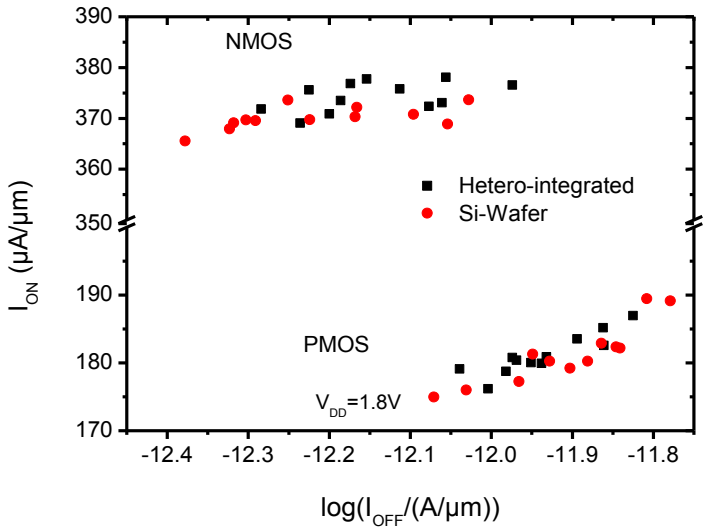



**Figure 7: On- and Off-current of a standard MOS transistor structure with a nominal gate length of 0.24 µm and a gate width of 25 µm.**

Figure 7 shows a comparison of $I_{ON}$ vs $I_{OFF}$ characteristics of the 1.8V CMOS transistors for the standard MOS structure with a gate length of 240 nm and a gate width of 25 µm. No difference before and after hetero-integration can be observed.
In this way all relevant parameters were assessed with the result that there is no influence on the CMOS parameters. We can conclude there is no impact on the CMOS parameters caused by the hetero-integration process.

### 3.3.2 The DC characteristics of the SiGe-HBTs

The SiGe-HBT transistors were tested before and after completion of the wafer-bonding and finalization of the InP HBT layer stack, including the Au metallization as described in [Kraemer 2013] to assess the influence of the heterogeneous integration on these devices, as well.

A Gummel plot of the transistor npn2 is shown in Figure 8. This transistor has a drawn emitter area of 0.18 x 0.48 µm$^2$ and is optimized for a high maximum oscillator frequency value. The calculated common-emitter current gain β is shown on the right y-axes in Figure 8. The gain of the hetero-integrated device is smaller for voltages lower than 0.7 V. This is caused by an increased base current in this voltage range, whereas the collector current is unaffected by the hetero-integration process.

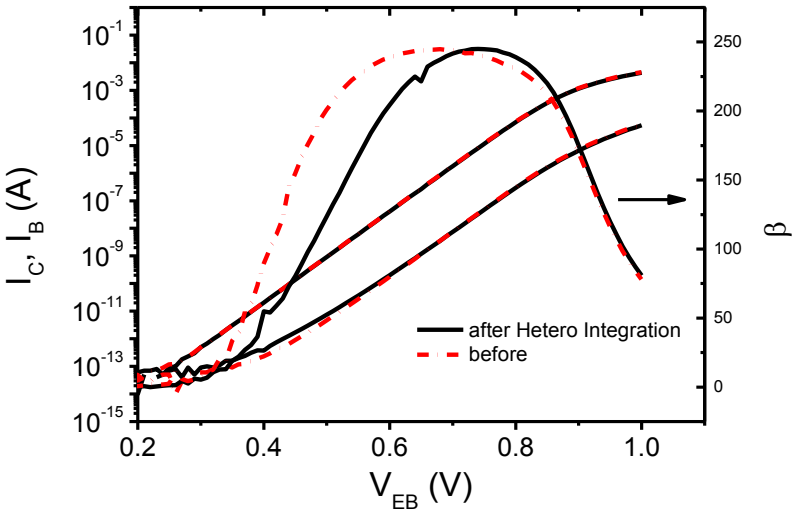



**Figure 8: Gummel plot before and after hetero-integration for npn2**

### 3.3.3 The RF characteristics of the SiGe-HBTs

The RF performance of the HBTs is very important to enable integrated circuits with high operating frequencies. Possible changes in the high frequency performance of these devices should be considered for the design of hetero-integrated circuits. These measurements were also performed to verify transistor models in hetero-integrated design kit. One part of the process control monitors is the section for RF testing of the HBTs. The test structures include two different SiGe BiCMOS transistors npn1 and npn2 in ground-signal-ground configuration as well as the corresponding de-embedding structures.
As described earlier, the RF performance of the transistors was initially recorded after finishing the top-metal-2 (TM2) layer. We measured the current gain cutoff frequency $f_T$ and unilateral gain cutoff frequency $f_{max}$ values in a checkerboard arrangement (every second die) because of the enormous number of dies on a 200 mm wafer. For our standard test program the $f_T$- and $f_{max}$-values are extrapolated from measurements at 30 GHz using an Agilent 8510C vector network analyzer as the measurement tool. The results are summarized in the following Table 4. The changes of current gain cutoff frequency $f_T$ and of unilateral gain cutoff frequency $f_{max}$ due to the heterointegration process are in the range of a few GHz and negligible.

**Table 4: $f_T$ and $f_{max}$ for the two HBTs**

| | **npn1** | | **npn2** | |
|---|---|---|---|---|
| | 200mm | 3" HI | 200mm | 3" HI |
| Mean $f_T$ | 175 GHz | 176 GHz | 172 GHz | 174 GHz |
| Sigma wafer | 7.0 GHz (4.0%) | 2.1 GHz (1.2%) | 7.4 GHz (4.3%) | 2.2 GHz (1.3%) |
| Range wafer | 25.3 GHz (14.5%) | 7.6 GHz (4.3%) | 26.8 GHz (15.6%) | 7.8 GHz (4.5%) |
| Mean $f_{max}$ | 180 GHz | 178 GHz | 198 GHz | 195 GHz |
| Sigma wafer | 2.7 GHz (1.5%) | 4.1 GHz (2.3%) | 2.7 GHz (1.4%) | 2.6 GHz (1.3%) |
| Range wafer | 12.8 GHz (7.1%) | 9.3 GHz (5.2%) | 14.5 GHz (7.3%) | 10.8 GHz (5.5%) |

Figure 9 shows the current-mode logic type (CML) ring oscillator gate delay □$_D$ as a function of the current per gate for the two different HBT transistors before and after hetero-integration. There are nine different ring oscillators on every die. Four ring oscillators based on npn1 and five for npn2. The ring oscillator consists of 53 transistor stages in series. The ring oscillators differ in terms of the load resistors. The lowest value of the gate delay time was reached for the ring oscillator with about 0.6 mA current per gate for both types of transistors. The curves with solid lines and symbols represent the ring oscillators for the hetero-integrated 3" wafer, whereas the dashed line with the open symbols denote the 200 mm Si wafer. The measured gate delay time for the HBT npn2 on the 200 mm wafer is 4.30 ps for a current per gate of 0.63 mA. The smallest measured gate delay time for npn2 on a 3" hetero-integrated wafer is 4.36 ps for a current per gate of 0.65 mA. There is a shift of 0.06 ps, which corresponds to a change of 1.4%.

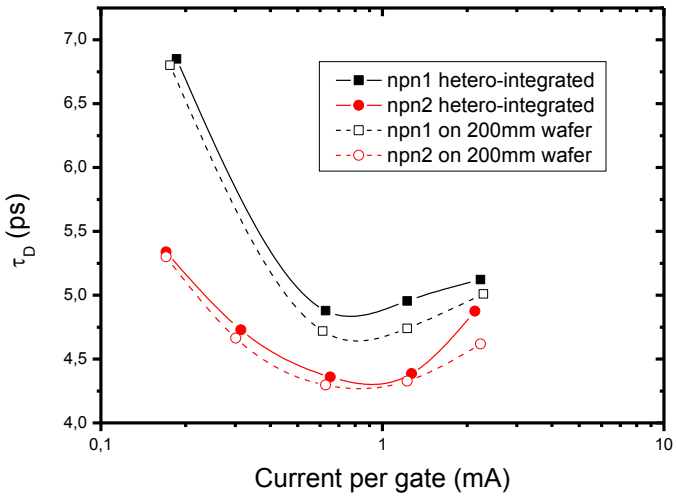



**Figure 9: Ring oscillator gate delay $\tau_D$ as a function of the current per gate**

The homogeneity over the wafer was checked by measuring the ring oscillator circuit with the shortest gate delay time on each single die. The results are shown in Figure 10. The yield of this oscillator circuit including more than 160 transistors each is almost 100%. Only at the very edge of the wafer the measurement fails. The mean value for that typical wafer is 4.336 ps with a standard deviation of 0.053 ps, which corresponds to a maximum oscillator frequency of 230 +/- 8 GHz (8GHz = 3σ□□□□□□□□□□□□□□Figure 10. For a hetero-integrated 3" wafer the gate delay is 4.336 ps with a standard deviation of 0.013 ps, corresponding to 0.3%. The range is 0.04 ps (1%) which is an excellent value (see Figure 11).

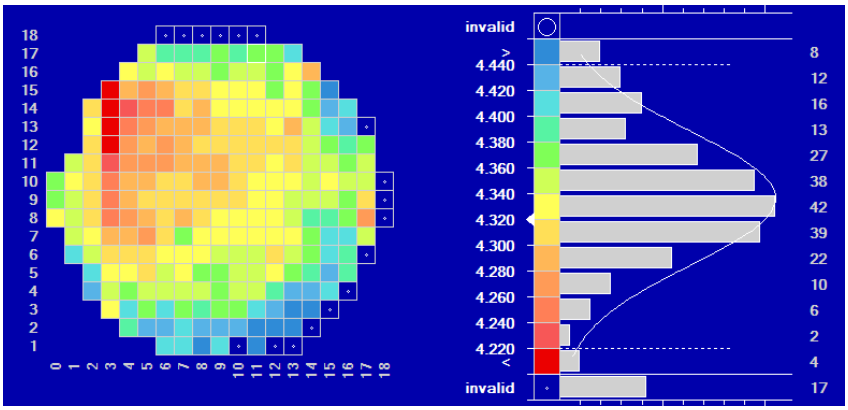



**Figure 10: Distribution of measured CML ring oscillator gate delay time of npn2 over one 200 mm wafer. The unit is ps. The mean value is $\tau_D$ = 4.336 ps, the standard deviation is σ = 0.053 ps.**

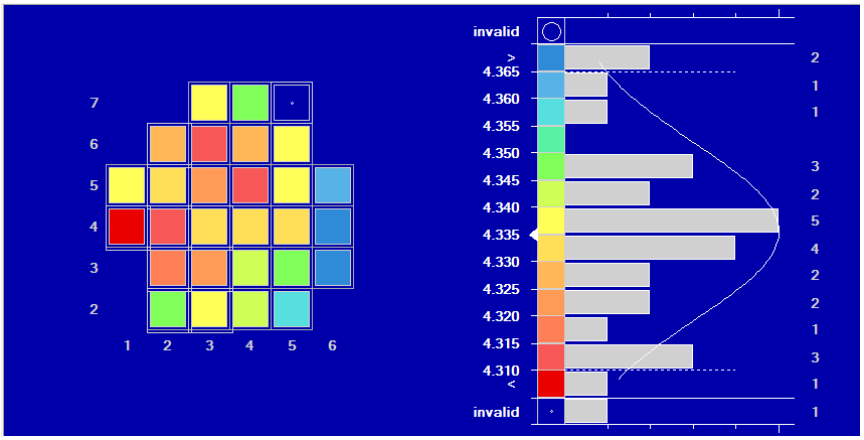
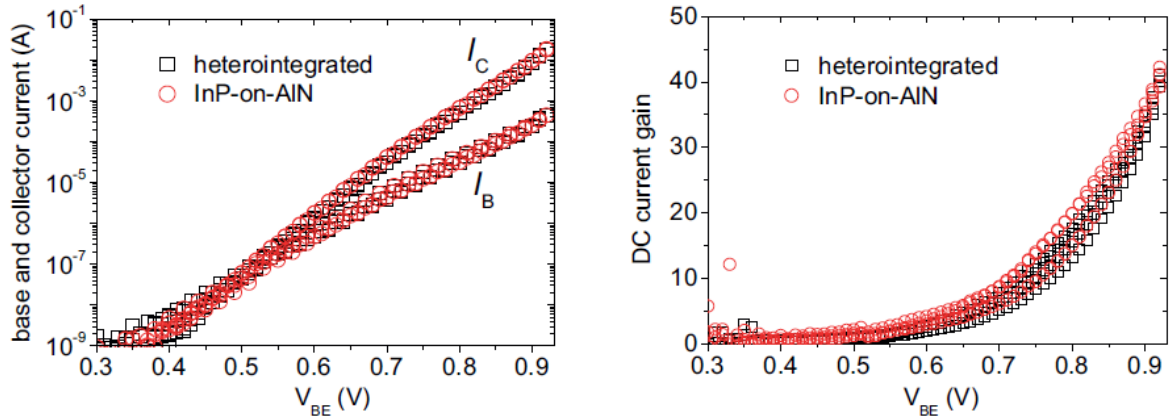



**Figure 11: Distribution of measured CML ring oscillator gate delay over one 3" wafer. The mean value is $\tau_D$ = 4.336 ps, the standard deviation is σ = 0.013 ps.**

In conclusion, it can be stated that the BiCMOS device performance is kept practically unchanged by the heterointegration process, coming from the fact that the BiCMOS processing sequence remained almost the same, and the heterointegration includes only processes with temperatures below 250°C.

### 3.4 InP DHBTs

InP and Si have a significant difference in the thermal expansion coefficient (CTE), 4.6 x $10^{-6}$ $K^{-1}$ for InP and 2.6 × $10^{-6}$ $K^{-1}$ for Si, which leads to a mechanical stress during wafer bonding probably leading to a deterioration of the InP epitaxial layer stack.
The ideality factors of a pn-diode and reverse leakage currents of silicon hetero-integrated InP HBT diodes with the InP-on-AlN standalone transfer substrate process can be used to evaluate the material properties for different approaches. When comparing the crossover point of base and collector current in the Gummel plot, the DC current gain, and the slope of the collector and base current curves, there is just a little difference between both technologies (see Figure 12). This indicates that the InP HBT "islands" are completely relaxed at the completion of the integrated process.




a) Base and collector currents.

b) DC current gain.

**Figure 12: Gummel plots on heterointegrated and InP-on-AlN InP DHBTs**

The cutoff frequencies in Figure 13 were computed without device de-embedding. When subtracting the parasitic circuit elements of the test frame and probe pads, $f_T$ rises by ≈50 GHz and $f_{max}$ by ≈10 GHz. The maximum small signal gain occurs at a collector current of 25mA for the single-finger 0.8 × 6.0 $\mu m^2$ InP DHBT, and at 40mA for the double-finger design

with 2 × 0.8 × 6.0 µm$^2$ emitter area. The standard deviation of $f_T$ and $f_{max}$ of functioning devices lies within 2 and 5%, respectively.
We measured wafer maps of the same device geometry on 37 dies on a four-wafer lot with 3" diameter. The overall cut-off frequency statistics of functioning devices with single- and double-finger geometry is given in Figure 13.

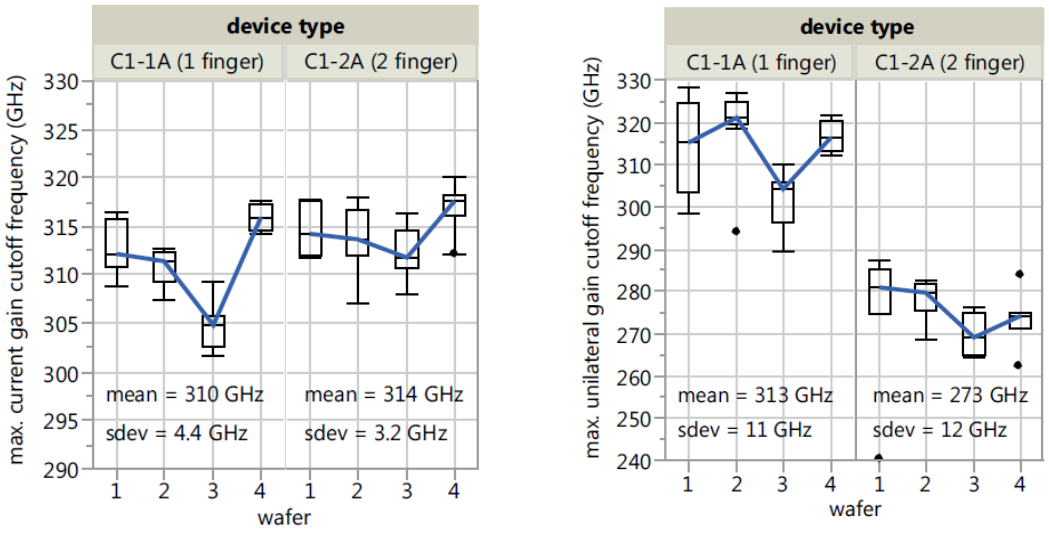



**Figure 13: Distribution of current gain cutoff frequency $f_T$ and of unilateral gain cutoff frequency $f_{max}$ over a four-wafer lot**

### 3.5 InP DHBT Technology Issues

The recorded wafer yield of InP DHBTs is approximately 80%. The yield is affected by rather large-diameter BCB defects, which locally disturb the planarization height and hence may lead to device-open or device-short errors. The yield impact is not randomly located, but is clustered at these defect sites. Otherwise, it would not be possible to produce functioning circuits with more than ten transistors. The increase of the yield and the transition from 3" to 4" in wafer size are goals in future propositions to improve the cost structure.
The InP DHBT module as an add-on is mainly targeted to analog mm-wave applications. Current and future developments include DHBT devices with higher cut-off frequencies through geometrical scaling. The SciFab is currently the only hetero-integrated semiconductor technology, which produces circuits with output frequencies above 100 GHz. But it has still several restrictions that limit the applications related to the cutoff frequencies of 0.8 microns InP HBTs, and the available output power.
The reduction of the emitter width from 0.8 µm to 0.5 µm can be beneficial and will lead to the increase of $f_{max}$ of hetero integrated InP-DHBT transistors to at least 500 GHz, and thus enables the realization of amplifiers and active mixers at 250 GHz.
There are some applications, which require a low noise figure of the InP DHBT devices, e.g. low noise amplifiers. The noise measurements of our 0.8 µm DHBT results in a noise figure of 5 dB at these frequencies. A reduction of the emitter area will also positively influence the noise figure of the DHBT devices. Efficient low noise amplifiers will then be feasible in the InP DHBT technology and might be hetero-integrated with SiGe BiCMOS circuit building blocks.
A more serious concern for such a technology platform is the reliability. In the current state of the development the InP DHBTs shows a very rapid degradation after operating at standard conditions. A possible reason might be a defective semiconductor surface passivation consisting of benzocyclobutene (BCB) and improvements maybe reached by using silicon nitride or aluminum oxide layers instead.

### 3.6 Demonstrator Circuits

Due to the alignment accuracies given by the alignment tools the heterointegration scheme consists of one or more InP DHBT and SiGe BiCMOS sub-circuits. These sub-circuits are connected via RF microstrip transitions between the InP and the BiCMOS metallization systems.
The base for all developed signal sources are IHP's voltage controlled oscillators with different output frequencies with and without phase locked loop (PLL) control circuitry. The 82 GHz VCO is the most frequently used source in the project. The oscillator is based on a differential Colpitts topology, which is a widespread choice in mm-range VCOs for low phase noise applications [Wang 2008]. The output spectrum is shown in Figure 14.

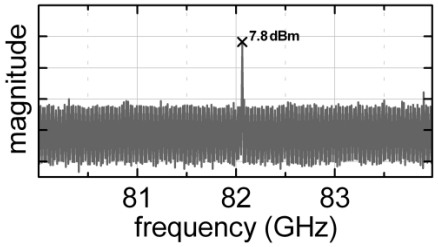



**Figure 14: Output spectrum of an 82 GHz VCO on the InP-on-BiCMOS wafer**

The lower the impact of the heterogeneous integration is on the BiCMOS circuit performance, the more viable is the sharing of validated circuit libraries. Measurements at the same stand-alone VCO layouts were performed over three different BiCMOS wafers. The results are summarized in Table 5.

**Table 5: Frequency and output power of the 82 GHz VCO with and without hetero-integration under the same bias conditions**

| | **wafer center not hetero-integrated** | **low right quarter not hetero-integrated** | **low right quarter hetero-integrated** |
|---|---|---|---|
| Mean f | 83.82 GHz | 83.42 GHz | 82.10 GHz |
| Standard deviation over the 3" wafer | 0.067 GHz (0.08%) | 0.083 GHz (0.1%) | 0.081 GHz (0.1%) |
| Mean output power | 5.9 mW | 6.6 mW | 6.0 mW |
| Standard deviation over the 3" wafer | 0.08 mW (1.3%) | 0.39 mW (6%) | 0.62 mW (8%) |

One wafer being heterogeneously integrated shows an average output power Pout = 6.0 mW ± 0.62 mW (8%) at averaged frequency f = 82.1 GHz ± 0.81 GHz (0.1%) right column in Table 5. The corresponding control sample of circuit from a quarter of a 200 mm BiCMOS wafer from the same lot without heterogeneous integration shows an output power Pout = 6.6 mW ± 0.39 mW (6%) at frequency f = 83.42 GHz ± 0.83 GHz (0.1%) under identical bias condition. The values of output power and its deviation are quite similar.
This moderate variance of ~1.5 GHz marks the upper limit of the potential influence from the heterogeneous integration on the employed BiCMOS circuits. A tunable frequency range for the heterogeneous integrated VCO of 81.8–82.4 GHz could be determined with <0.2 dB variation in the output power.

Another measurement for a 3" wafer originated from the 200mm wafer center shows a standard deviation of 0.08% for the output frequency and 1.3% for the output power of the

VCO. That highlights the very low variance of the devices in the BiCMOS technology. The yield of functioning circuits was almost 100%.

This BiCMOS VCO was used to realize hetero-integrated signal sources.
The VCO of the combined circuit operates at approximately 82 GHz with an output power of 7.8 dBm (6 mW), while the doubler-amplifier chain delivers 0 dBm at 164 GHz [Jensen 2013]. This 164 GHz signal source represented the first heterogeneous integrated circuit, operating at mm-wave frequencies and demonstrated the ability of this new circuit class to operate well above 100 GHz in the milliwatt range. The publication was honored with the best paper award at EuMIC 2013. A redesign of this circuit (VCO + frequency doubler + amplifier) within the SciFab runs shows an output power of +7.0 dBm which corresponds to 5 mW [Jensen 2014].
Another combination of circuit building blocks realized in this project is a combination of the 82 GHz VCO with an InP-based frequency tripler. The RF transition takes place at 82 GHz.
The overall chip area is 3 × 1 mm². DC biasing of the voltage control oscillator on BiCMOS as well as that of the tripler on InP DHBTs is all done through DC pads on the InP metallization layer (right in Figure 15). About -10 dBm power is obtained at 246 GHz. The power levels of the fundamental and second harmonic signals at the output are low due to suppression by a band pass filter at the output. This tripler circuit was redesigned and processed in a following run. The output power was increased to -1.6 dBm.
Also a quadrupler circuit was realized in InP and coupled to the 82 GHz BiCMOS VCO. The quadrupler included a balun realized in the InP module. The quadrupler is followed by a differential InP DHBT buffer amplifier stage. The measured output power is -12 dBm which corresponds to 0.06 mW.

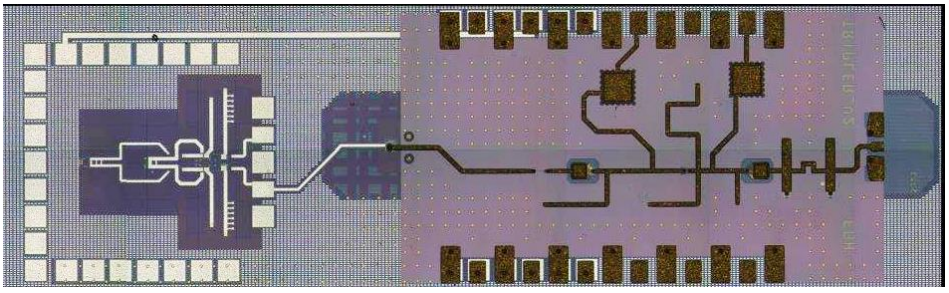


**Figure 15: Chip photograph of the Hetero Integrated Circuit.**

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## 4. Foundry Access

The SciFab foundry access is enabled through IHP's multi-project-wafer MPW user interface. Potential customers can request the design kit from IHP as the tool kit for designing their own circuits. Tested functional circuit building blocks are also available on request. Design submission is equal to IHP's BiCMOS processes – customers submit their final GDS file and after checking the layouts the wafer preparation is started at IHP followed by the processing at the FBH. The requested number of chips is shipped after the completion of the fabrication process to the customer. The SciFab InP/BiCMOS heterogeneously integrated foundry is currently operating in an early access mode with a selected number of external customers.

## 5. Conclusion

The SciFab project leads to a hetero-integrated InP DHBT on SiGe BiCMOS technology which is opened up to-third party customers in a foundry mode. An InP-DHBT module with 800 nm emitter width devices is added to IHP's qualified 250 nm BiCMOS technology.
Due to the marginal influence of the hetero-integration on the SiGe devices the transistor models for the SiGe devices in the design kit remain valid. The design kit was extended to include the models of the InP HBTs and passives included in the BCB – gold back-end-of-line stack of the InP technology.
The hetero-integrated InP DHBT devices showing de-embedded $f_T$ and $f_{max}$ values of 360 and 330 GHz. The collector currents at the maximum frequency of the single and double emitter transistors were 25 mA and 40 mA, respectively, showing the capabilities of these devices.
Demonstrator circuits consisting of InP DHBT and SiGe BiCMOS building blocks connected via a special designed, low-loss RF transition showing promising results even at their first production cycle. The results in terms of power output were always improved by a second re-designed layout, which shows the potential of the hetero-integrated technology. Nevertheless further improvements in particular for the fully integrated InP-devices have to be achieved to benefit sufficiently from this novel heterogeneous technology platform.
The goal of the SciFab project was to enhance networking between the Leibniz institutes IHP and FBH on the topic of heterogeneous material integration for electronic high-frequency applications. The most visible result of the improved interaction between both institutes is the availability of a common circuit design kit, which includes all individual parts of both technologies in one framework. Besides the design kit, adjustments to data and information exchange between the partnering institutes were made, in order to improve the shared fabrication flow. The proof of SciFab being a functioning wafer fabrication lies in the

availability of the foundry service for heterointegrated InP/SiGe mm-wave chips. Any customer may now order chips through IHP's foundry interface, which include the InP transistors as an add-on module. First external customers are currently sampling the technology.

## 6. Publications


N.G. Weimann, D. Stoppel, M.I. Schukfeh, M. Hossain, T. Al-Sawaf, B. Janke, R. Doerner, S. Sinha, F.-J. Schmückle, O. Krüger, V. Krozer, W. Heinrich, M. Lisker, A. Krüger, A. Datsuk, Ch. Meliani, B. Tillack,
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Physica Status Solidi A **213** (4) 909 (2016)

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